M5M4V64S20ATP-8, -10, -12

64M (4-BANK x 4194304-WORD x 4-BIT) Synchronous DRAM

PRELIMINARY

Some of contents are subject to change without notice.

DESCRIPTION

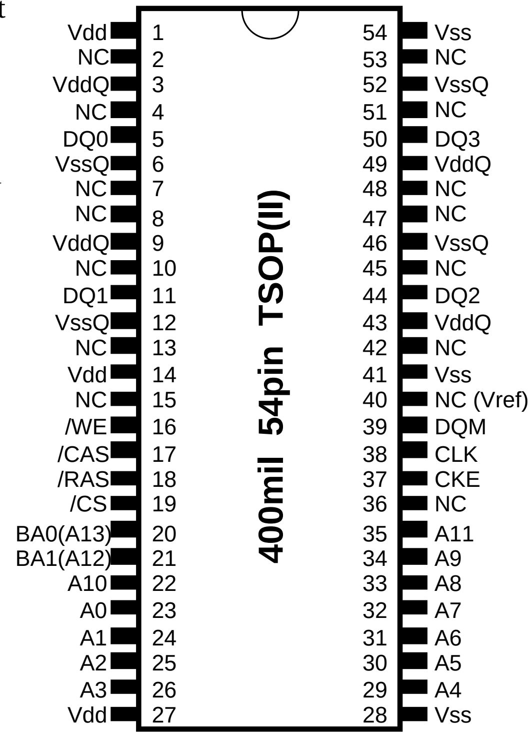
The M5M4V64S20ATP is a 4-bank x 4194304-word x 4-bit Synchronous DRAM, with LVTTL interface. All inputs and outputs are referenced to the rising edge of CLK. The M5M4V64S20ATP achieves very high speed data rate up to 125MHz, and is suitable for main memory or graphic memory in computer systems.

FEATURES

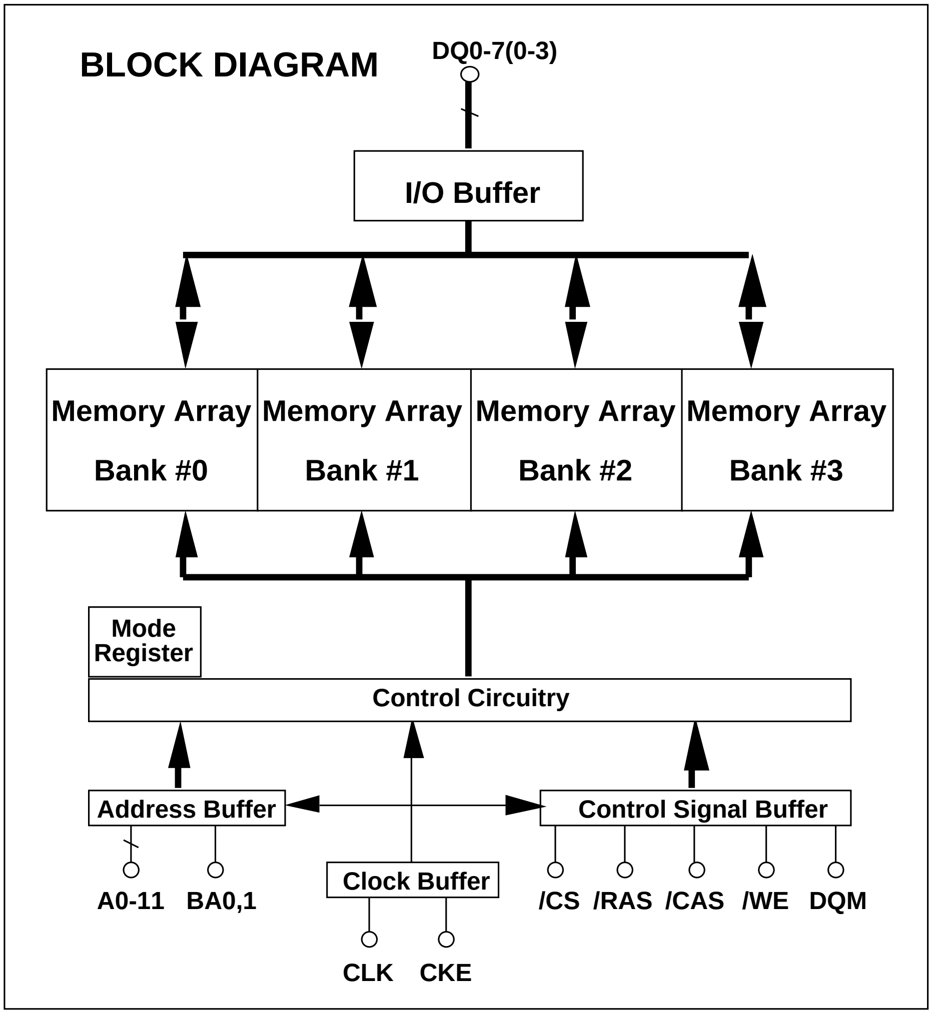
- Single 3.3v±0.3v power supply
- Clock frequency 125MHz / 100MHz / 83MHz
- Fully synchronous operation referenced to clock rising edge
- 4 bank operation controlled by BA0, BA1 (Bank Address)
- /CAS latency- 2/3 (programmable)
- Burst length- 1/2/4/8 (programmable)
- Burst type- sequential / interleave (programmable)
- Column access - random
- Auto precharge / All bank precharge controlled by A10
- Auto refresh and Self refresh
- 4096 refresh cycles /64ms
- Column address A0-A9
- LVTTL Interface
- 400-mil, 54-pin Thin Small Outline Package (TSOP II) with 0.8mm lead pitch

	Max. Frequency	CLK Access Time
M5M4V64S20ATP-8	125MHz	6ns
M5M4V64S20ATP-10	100MHz	8ns
M5M4V64S20ATP-12	83MHz	8ns

PIN CONFIGURATION (TOP VIEW)



CLK	**: Master Clock**
CKE	**: Clock Enable**
/CS	**: Chip Select**
/RAS	**: Row Address Strobe**
/CAS	**: Column Address Strobe**
/WE	**: Write Enable**
DQ0-3	**: Data I/O**
DQM	**: Output Disable/ Write Mask**
A0-11	**: Address Input**
BA0,1	**: Bank Address**
Vdd	**: Power Supply**
VddQ	**: Power Supply for Output**
Vss	**: Ground**
VssQ	**: Ground for Output**



Type Designation Code

This rule is applied to only Synchronous DRAM family.

M 5M 4 V 64 S 3 0 A TP - 8

- 8 — Cycle Time (min.) 8: 8ns, 10: 10ns, 12: 12ns
- TP — Package Type TP: TSOP(II)
- A — Process Generation
- 0 — Function 0: Random Column, 1: 2N-rule
- 3 — Organization 2n 2: x4, 3: x8, 4: x16
- S — **Synchronous DRAM**
- 64 — Density 64:64M bits
- V — Interface S: SSTL, V:LVTTL
- 4 — Memory Style (DRAM)
- 5M — Use, Recommended Operating Conditions, etc
- M — Mitsubishi Main Designation

PIN FUNCTION

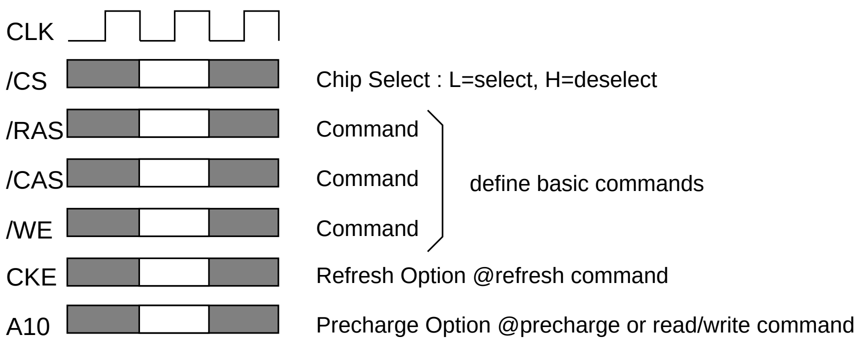
CLK	Input	Master Clock: All other inputs are referenced to the rising edge of CLK.
CKE	Input	Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
/CS	Input	Chip Select: When /CS is high, any command means No Operation.
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-11	Input	A0-11 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-11. The Column Address is specified by A0-9 (x4), A0-8 (x8). A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
BA0,1	Input	Bank Address: BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with ACT, PRE, READ, WRITE commands.
DQ0-7 (0-3)	Input / Output	Data In and Data out are referenced to the rising edge of CLK.
DQM	Input	Din Mask / Output Disable: When DQM is high in burst write, Din for the current cycle is masked. When DQM is high in burst read, Dout is disabled at the next but one cycle.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	VddQ and VssQ are supplied to the Output Buffers only.

BASIC FUNCTIONS

The M5M4V64S20ATP provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh.

Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /CS ,CKE and A10 are used as chip select, refresh option, and precharge option, respectively.

To know the detailed definition of commands, please see the command truth table.



Activate (ACT) [/RAS =L, /CAS =/WE =H]

ACT command activates a row in an idle bank indicated by BA.

Read (READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read (auto-precharge, **READA**).

Write (WRITE) [/RAS =H, /CAS =/WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA**).

Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 =H at this command, both banks are deactivated (precharge all, **PREA**).

Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE =H]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	BA0,1	A11	A10	A0-9
Deselect	DESEL	H	X	H	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X
Row Address Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V	V
Single Bank Precharge	PRE	H	X	L	L	H	L	V	X	L	X
Precharge All Banks	PREA	H	X	L	L	H	L	X	X	H	X
Column Address Entry & Write	WRITE	H	X	L	H	L	L	V	X	L	V
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	X	H	V
Column Address Entry & Read	READ	H	X	L	H	L	H	V	X	L	V
Column Address Entry & Read with Auto-Precharge	READA	H	X	L	H	L	H	V	X	H	V
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X	X
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	X
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	X
		L	H	L	H	H	H	X	X	X	X
Burst Terminate	TERM	H	X	L	H	H	L	X	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	L	V*1

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE:
1. A7-A9 =0, A0-A6 =Mode Address

FUNCTION TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE / PREA	NOP*4
	L	L	L	H	X	REFA	Auto-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	NOP
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
PRE - CHARGING	H	X	X	X	X	DESEL	NOP (Idle after tRP)
	L	H	H	H	X	NOP	NOP (Idle after tRP)
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	NOP*4 (Idle after tRP)
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after tRCD)
	L	H	H	H	X	NOP	NOP (Row Active after tRCD)
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RE-COVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
RE-FRESHING	H	X	X	X	X	DESEL	NOP (Idle after tRC)
	L	H	H	H	X	NOP	NOP (Idle after tRC)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after tRSC)
	L	H	H	H	X	NOP	NOP (Idle after tRSC)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care
BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No OPeration

NOTES:
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

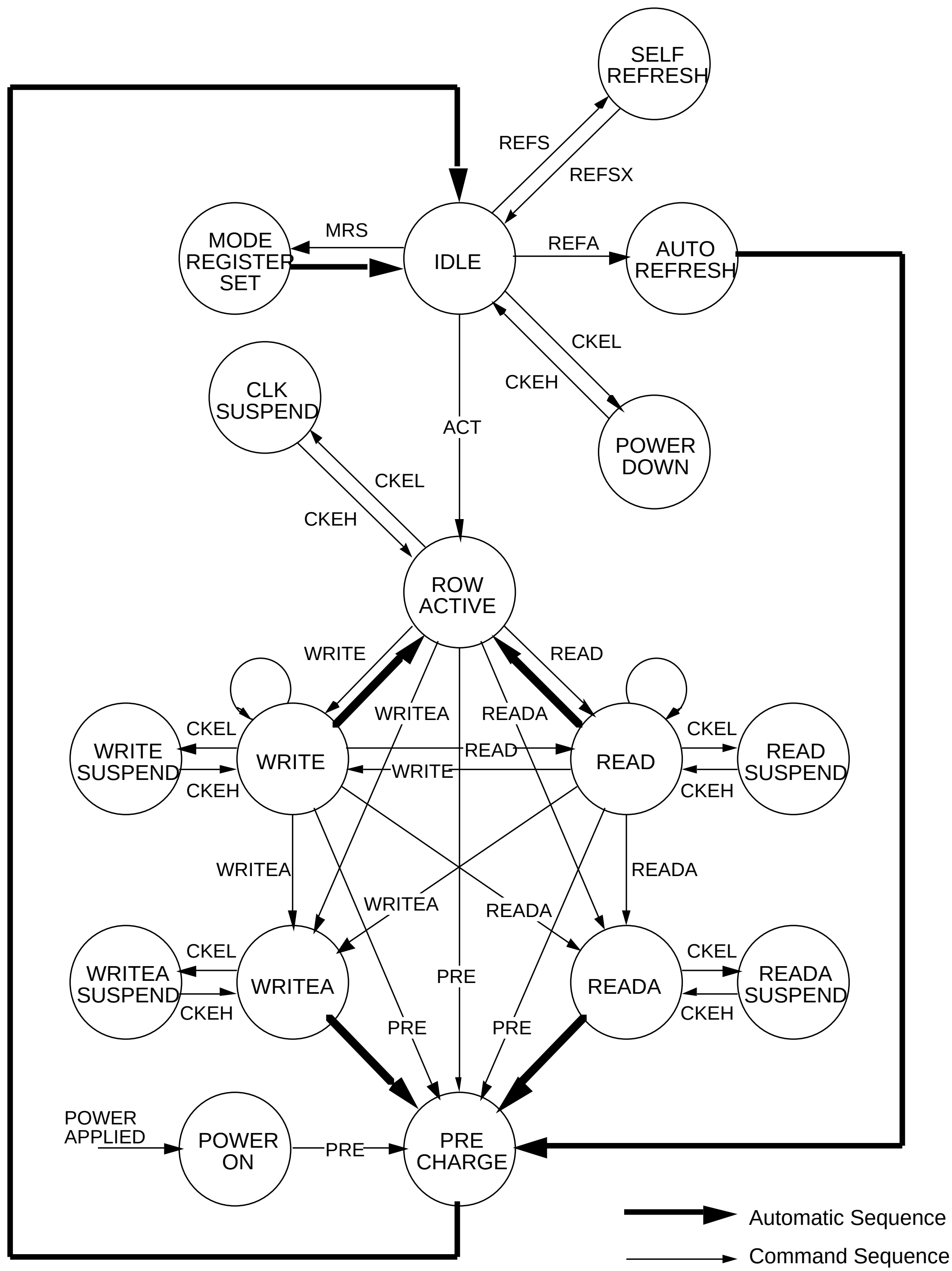
FUNCTION TRUTH TABLE for CKE

Current State	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	Add	Action
SELF-REFRESH*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State =Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CLK Suspend at Next Cycle*3
	L	H	X	X	X	X	X	Exit CLK Suspend at Next Cycle*3
	L	L	X	X	X	X	X	Maintain CLK Suspend

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care

NOTES:
1. CKE Low to High transition will re-enable CLK and other inputs **asynchronously**. A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

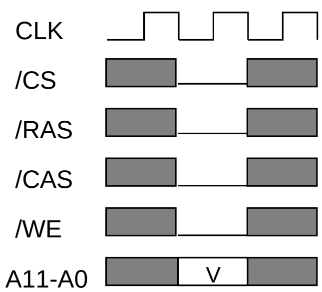
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQM high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 500µs.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when both banks are in@idle state. After tRSC from a MRS command, the SDRAM is ready for new command.



BA0	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	LTMODE			BT	BL		

LATENCY MODE

CL	/CAS LATENCY
0 0 0	R
0 0 1	R
0 1 0	2
0 1 1	3
1 0 0	R
1 0 1	R
1 1 0	R
1 1 1	R

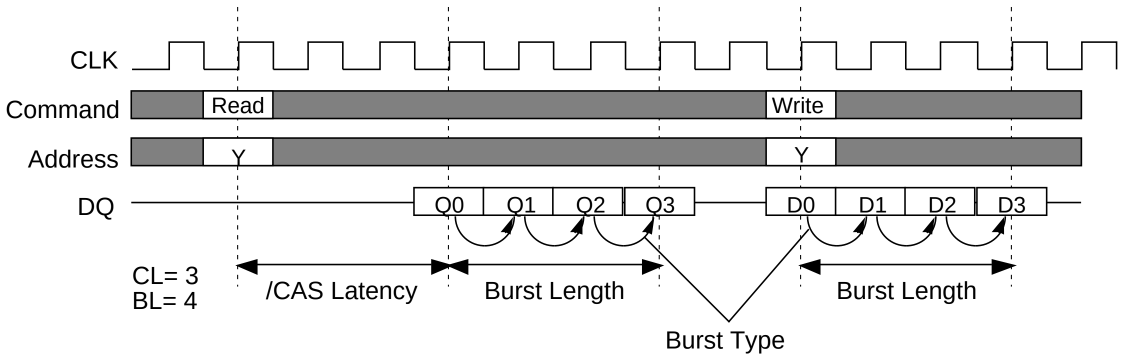
BURST LENGTH

BL	BT= 0	BT= 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	R	R
1 0 1	R	R
1 1 0	R	R
1 1 1	R	R

BURST TYPE

0	SEQUENTIAL
1	INTERLEAVED

R: Reserved for Future Use



Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

OPERATIONAL DESCRIPTION

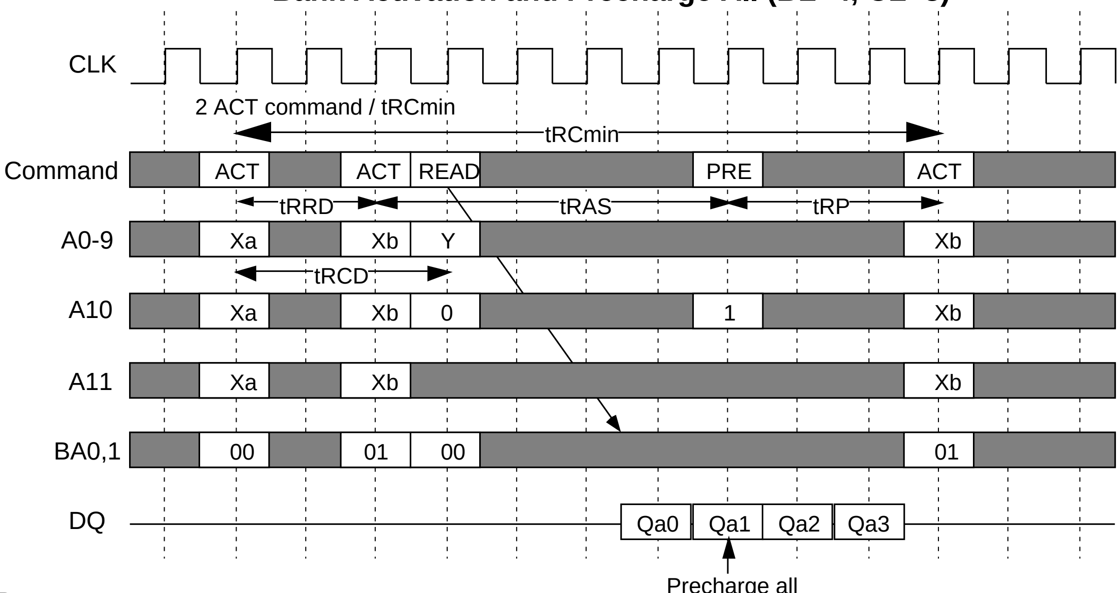
BANK ACTIVATE

The SDRAM has four independent banks. Each bank is activated by the ACT command with the bank addresses (BA0,1). A row is indicated by the row addresses A11-0. The minimum activation interval between one bank and the other bank is tRRD. *Maximum 2 ACT commands are allowed within tRC*, although the number of banks which are active concurrently is not limited.

PRECHARGE

The PRE command deactivates the bank indicated by BA0,1. When multiple banks are active, the precharge all command (PREA, PRE + A10=H) is available to deactivate them at the same time. After tRP from the precharge, an ACT command to the same bank can be issued.

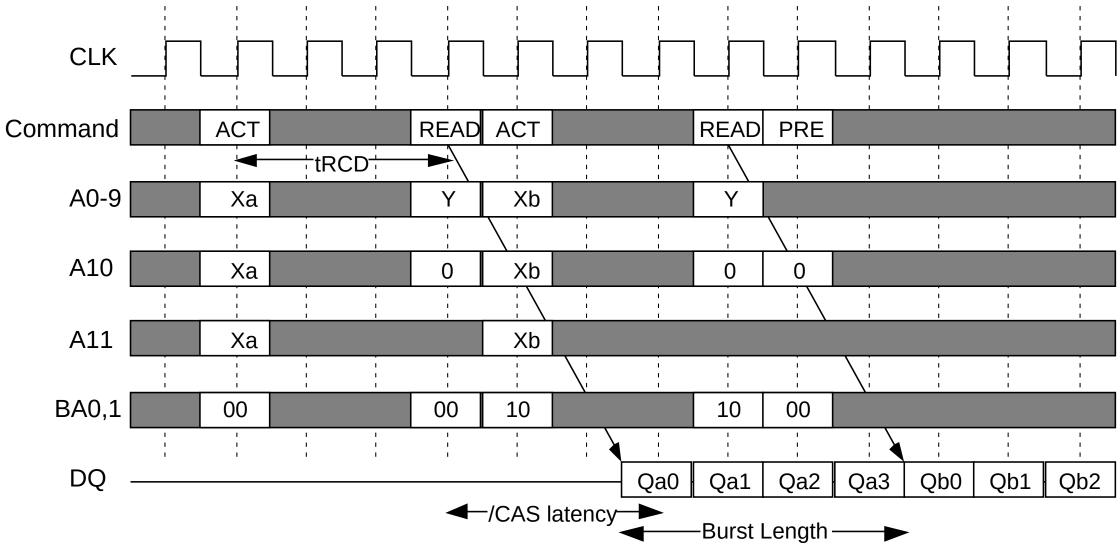
Bank Activation and Precharge All (BL=4, CL=3)



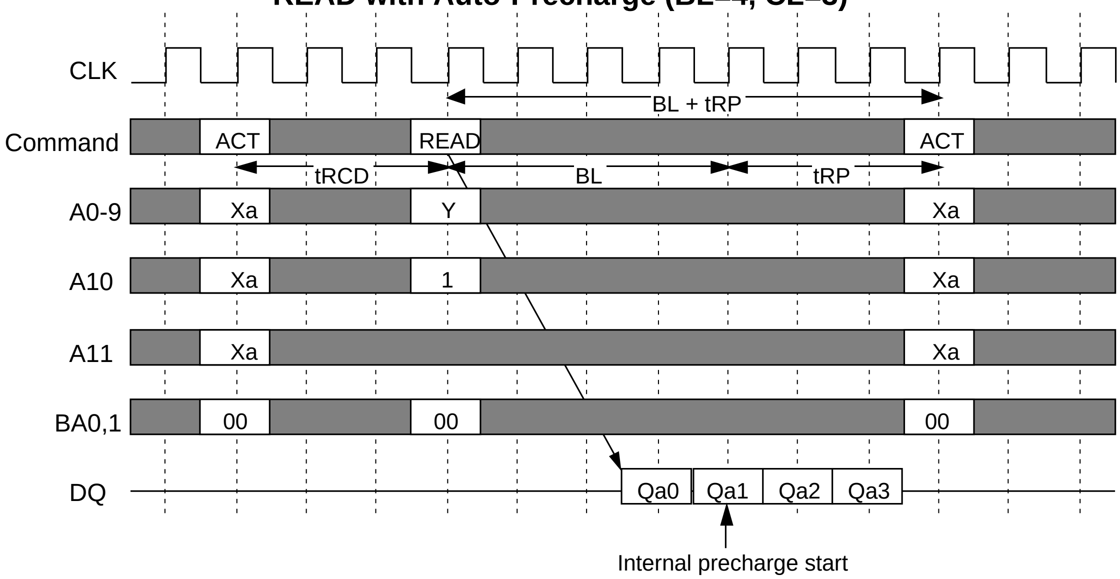
READ

After tRCD from the bank activation, a READ command can be issued. 1st output data is available after the /CAS Latency from the READ, followed by (BL -1) consecutive data when the Burst Length is BL. The start address is specified by A8-0 (x 8) / A9-0 (x 4), and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data by interleaving the multiple banks. When A10 is high at a READ command, the auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at BL after READA. The next ACT command can be issued after (BL + tRP) from the previous READA.

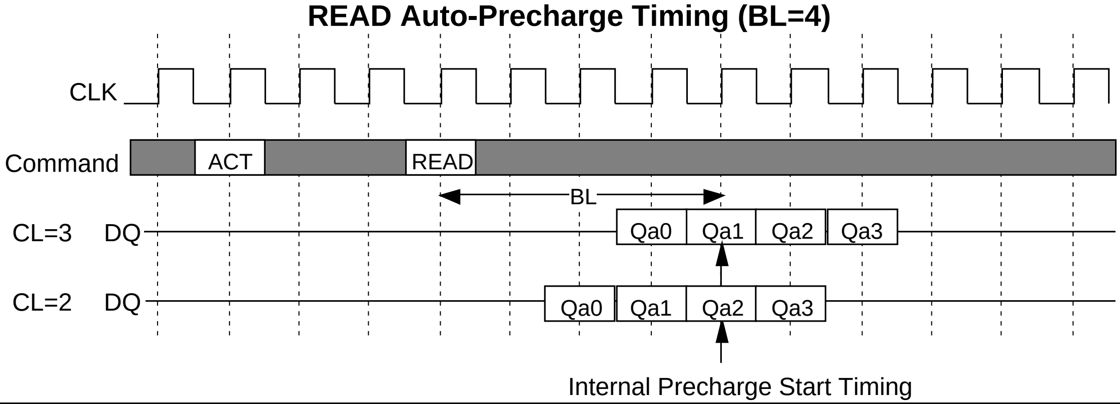
Multi Bank Interleaving READ (BL=4, CL=3)



READ with Auto-Precharge (BL=4, CL=3)



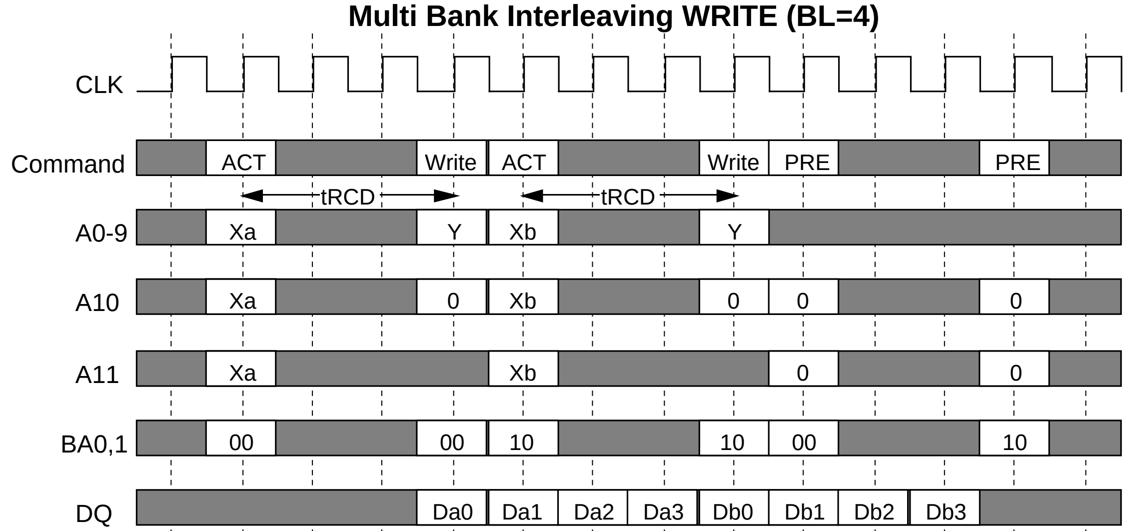
READ Auto-Precharge Timing (BL=4)



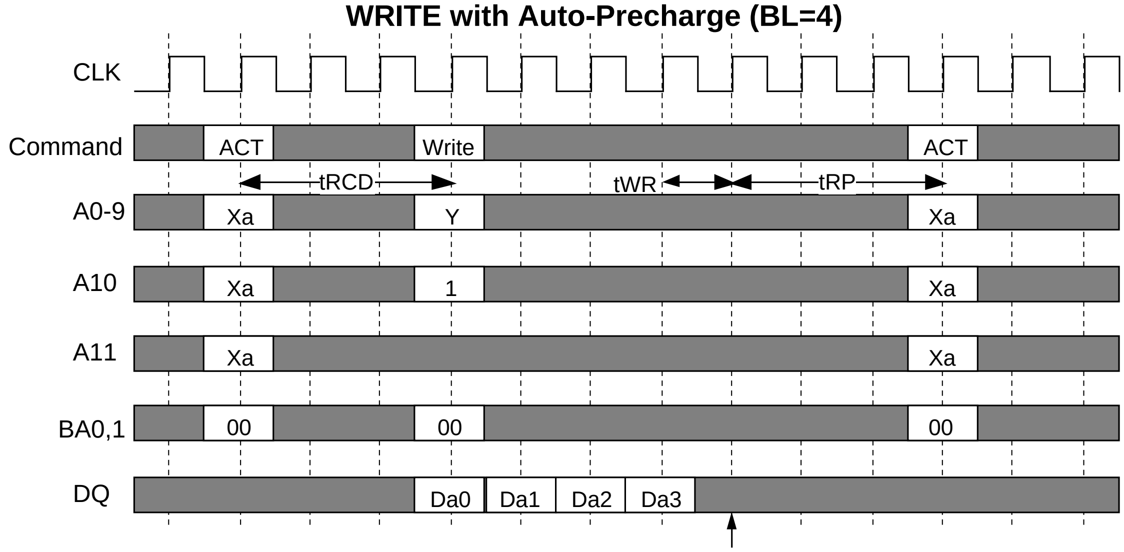
WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set at the same cycle as the WRITE. Following (BL -1) data are written into the RAM, when the Burst Length is BL. The start address is specified by A8-0 (x 8) / A9-0 (x 4), and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous input data by interleaving the multiple banks. From the last input data to the PRE command, the write recovery time (tWR) is required. When A10 is high at a WRITE command, the auto-precharge (WRITEA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge begins at tWR after the last input data cycle. The next ACT command can be issued after tRP from the internal precharge timing.

Multi Bank Interleaving WRITE (BL=4)



WRITE with Auto-Precharge (BL=4)

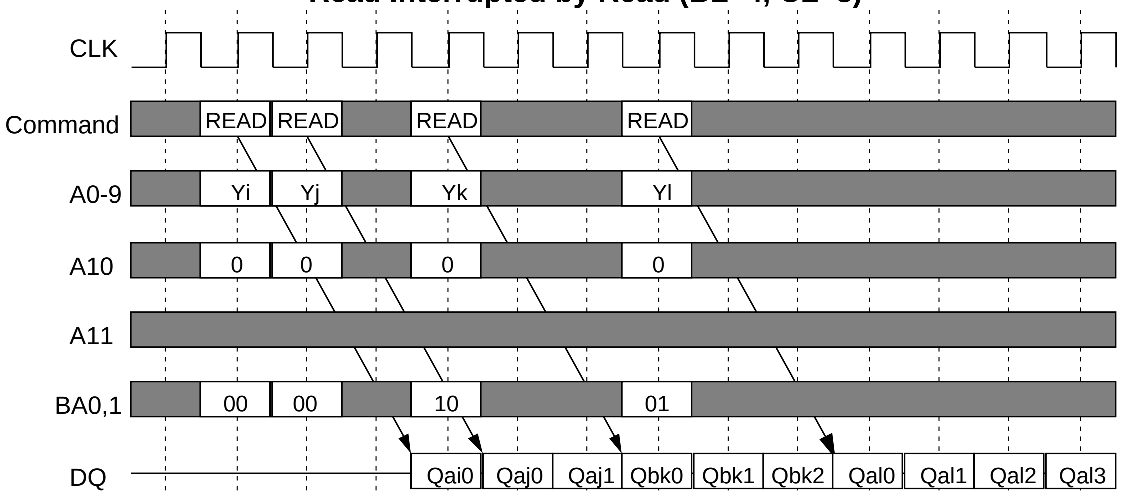


BURST INTERRUPTION

[Read Interrupted by Read]

Burst read operation can be interrupted by new read of any bank. Random column access is allowed. READ to READ interval is minimum 1 CLK.

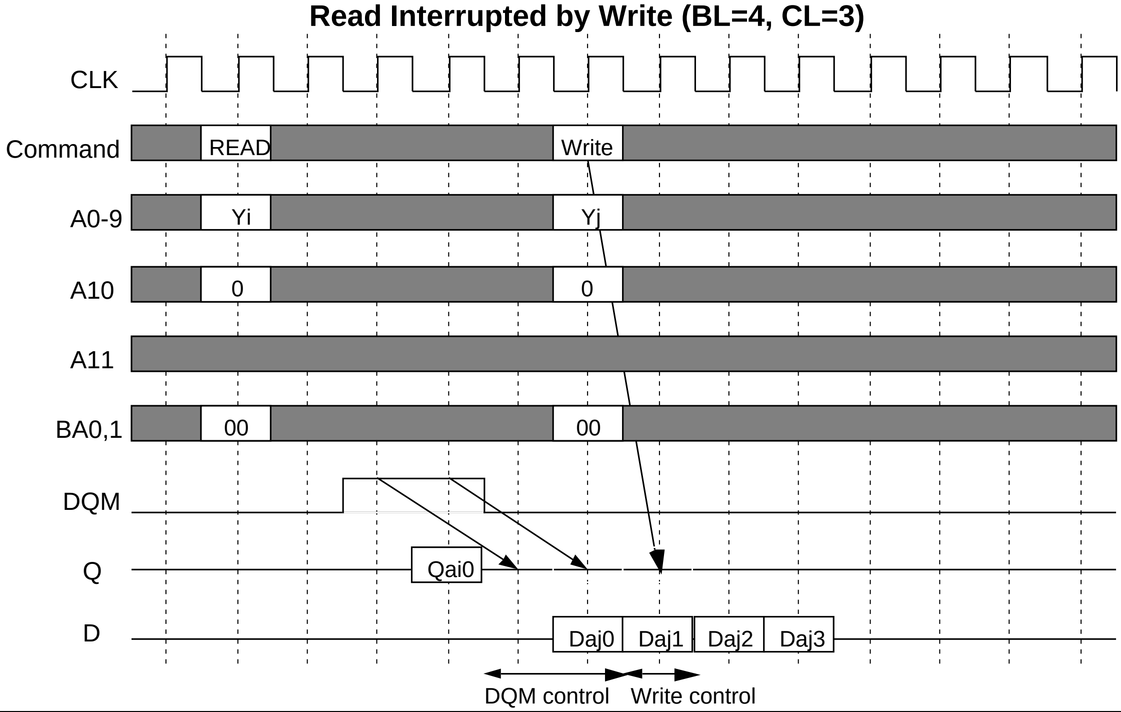
Read Interrupted by Read (BL=4, CL=3)



[Read Interrupted by Write]

Burst read operation can be interrupted by write of any bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQM to prevent the bus contention. The output is disabled automatically 1 cycle after WRITE assertion.

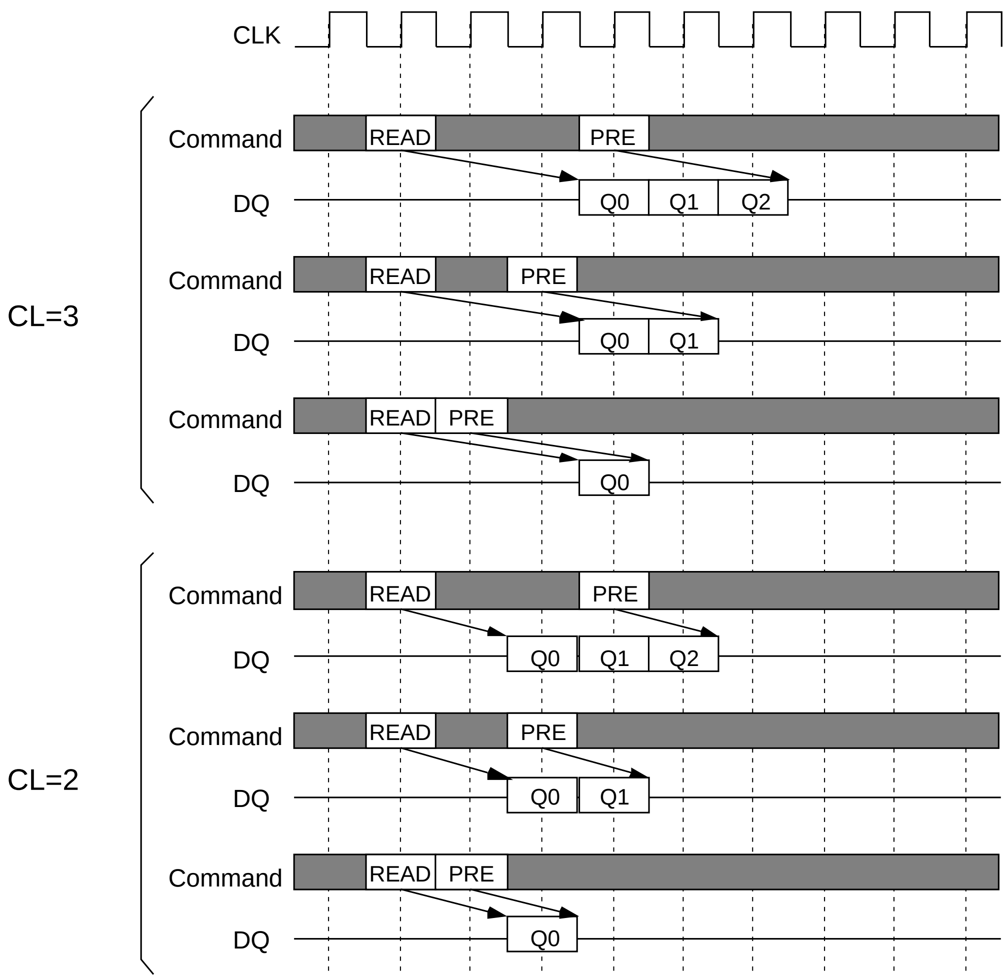
Read Interrupted by Write (BL=4, CL=3)



[Read Interrupted by Precharge]

Burst read operation can be interrupted by precharge of *the same bank*. READ to PRE interval is minimum 1 CLK. A PRE command to output disable latency is equivalent to the /CAS Latency. As a result, READ to PRE interval determines valid data length to be output. The figure below shows examples of BL=4.

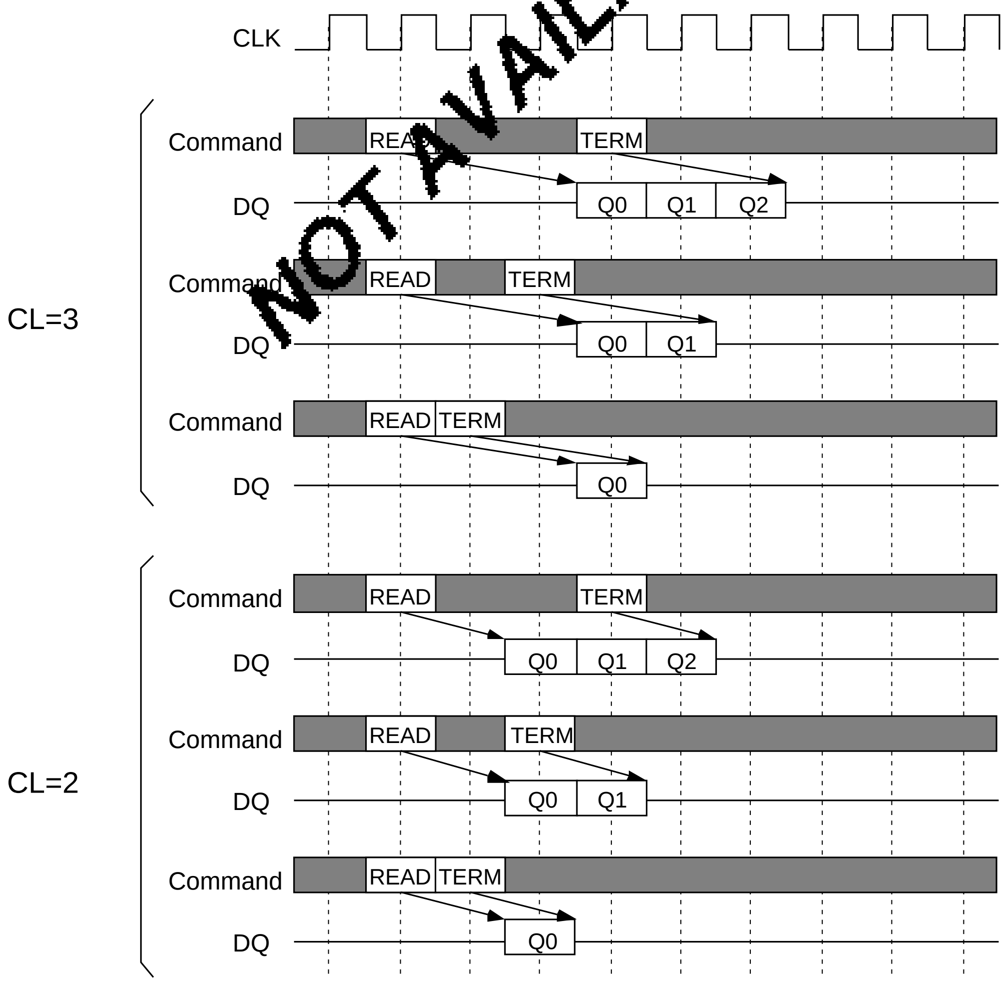
Read Interrupted by Precharge (BL=4)



[Read Interrupted by Burst Terminate]

Similarly to the precharge, burst terminate command can interrupt burst read operation and disable the data output. The terminated banl remains active. READ to TERM interval is minimum 1 CLK. A TERM command to output disable latency is equivalent to the /CAS Latency. As a result, READ to TERM interval determines valid data length to be output. The figure below shows examples of BL=4.

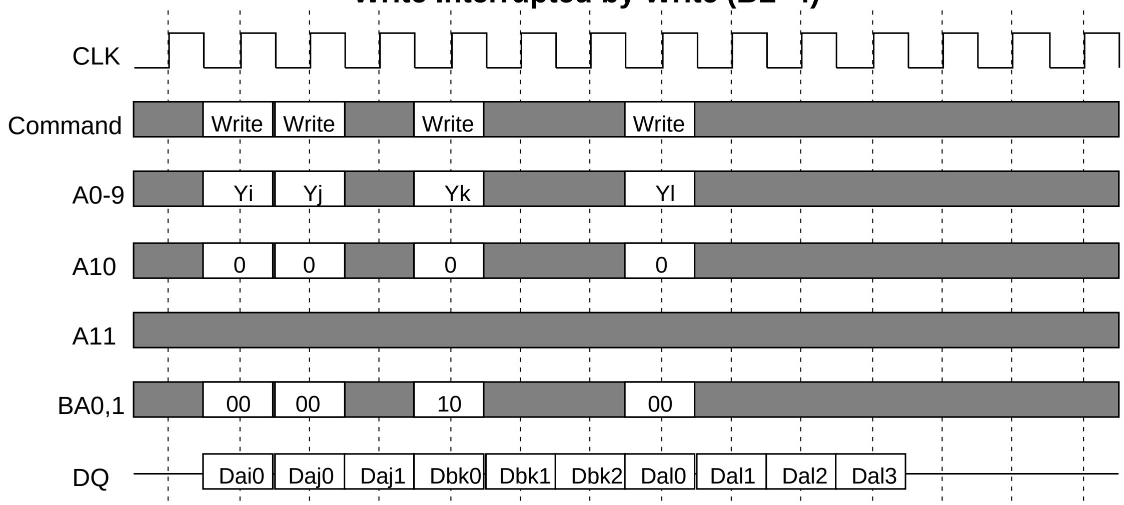
Read Interrupted by Burst Terminate (BL=4)



[Write Interrupted by Write]

Burst write operation can be interrupted by new write of any bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

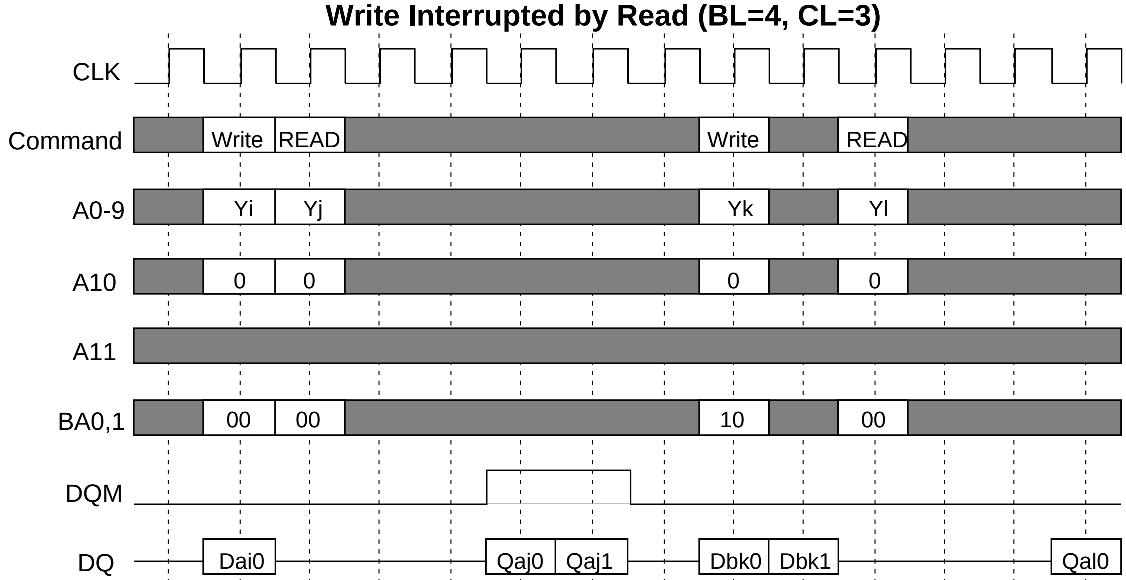
Write Interrupted by Write (BL=4)



[Write Interrupted by Read]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. WRITE to READ interval is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "don't care".

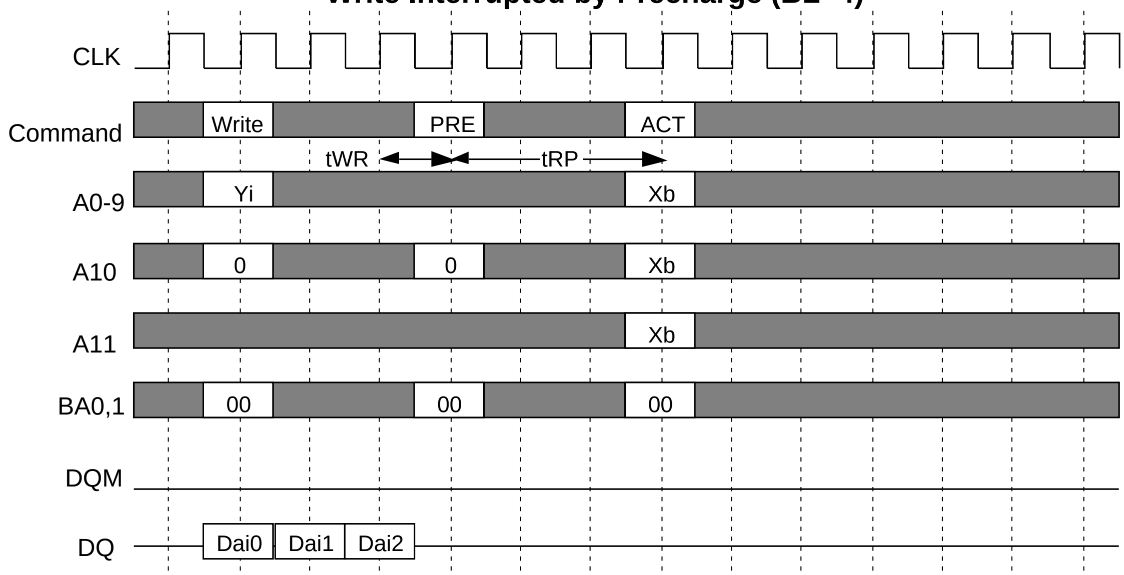
Write Interrupted by Read (BL=4, CL=3)



[Write Interrupted by Precharge]

Burst write operation can be interrupted by precharge of *the same bank*. Random column access is allowed. Write recovery time (tWR) is required from the last data to PRE command.

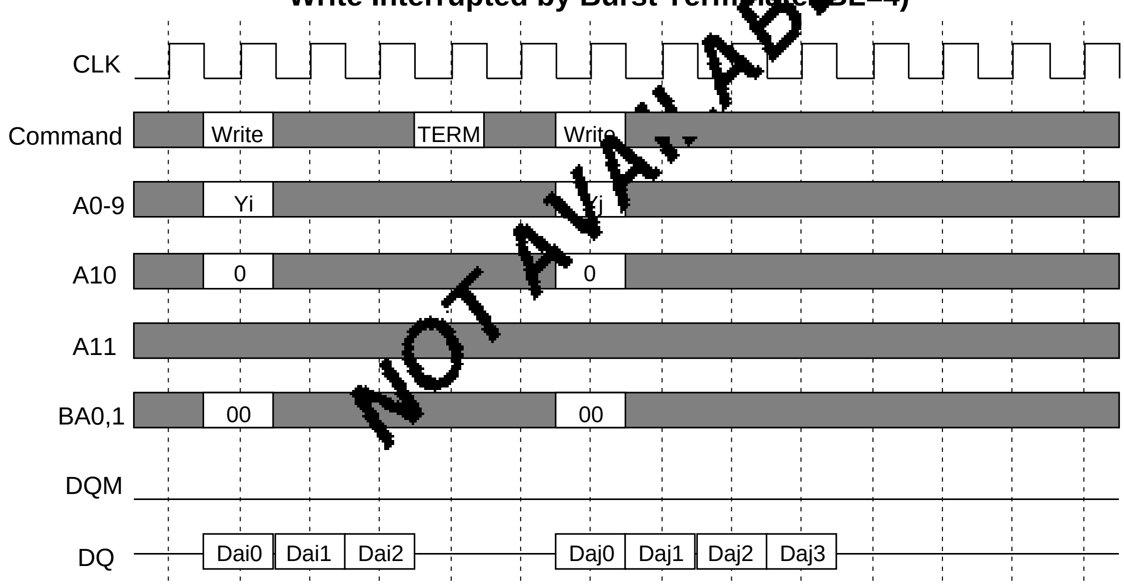
Write Interrupted by Precharge (BL=4)



[Write Interrupted by Burst Terminate]

Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. The figure below shows the case 3 words of data are written. Random column access is allowed. WRITE to TERM interval is minimum 1 CLK.

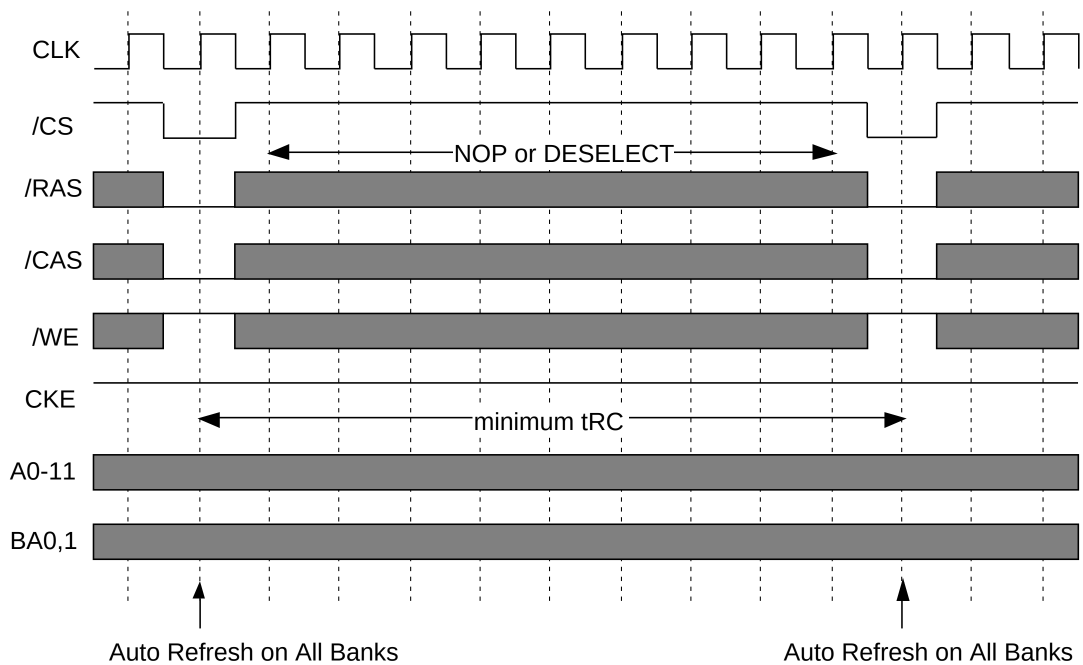
Write Interrupted by Burst Terminate (BL=4)



AUTO REFRESH

Single cycle of auto-refresh is initiated with a REFA (/CS= /RAS= /CAS= L, /WE= /CKE= H) command. The refresh address is generated internally. 4096 REFA cycles within 64ms refresh 64Mbit memory cells. The auto-refresh is performed on 4 banks concurrently. Before performing an auto-refresh, all banks must be in the idle state. Auto-refresh to auto-refresh interval is minimum tRC. Any command must not be supplied to the device before tRC from the REFA command.

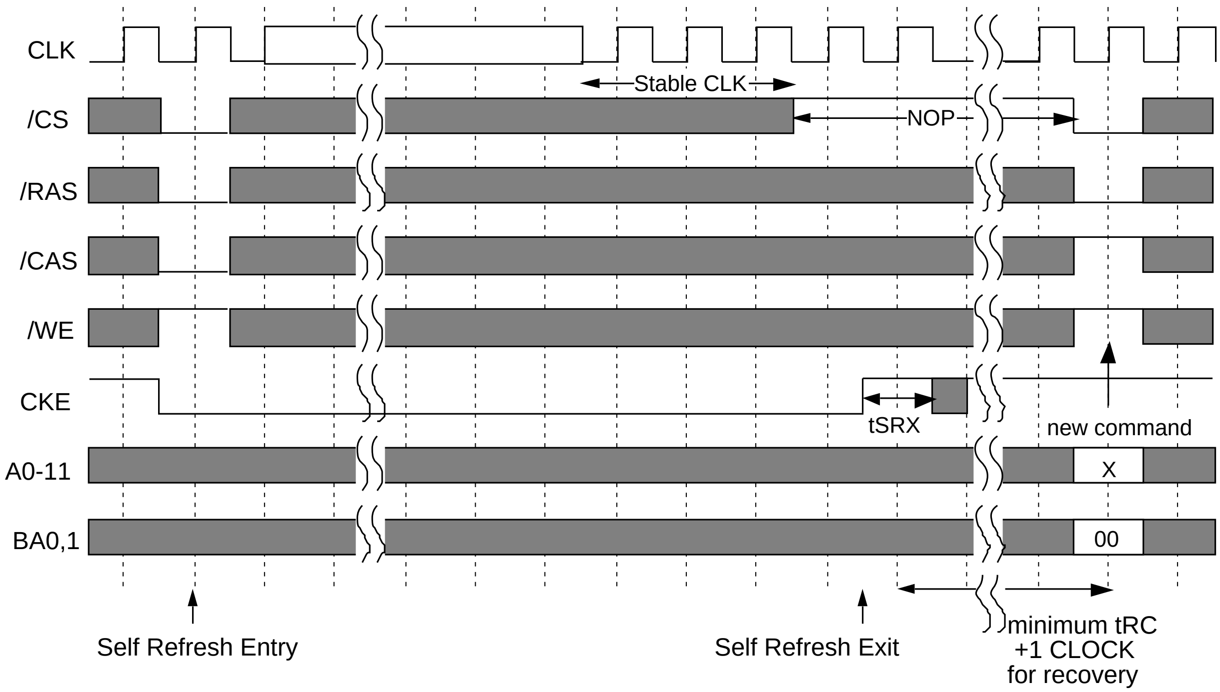
Auto-Refresh



SELF REFRESH

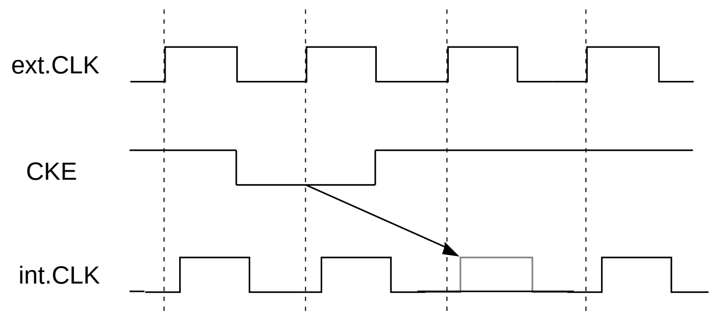
Self-refresh mode is entered by issuing a REFS command (/CS= /RAS= /CAS= L, /WE= H, CKE= L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enabled input ,all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE (REFSX) for longer than tSRX. After tRC from REFSX all banks are in the idle state and a new command can be issued, but DESEL or NOP commands must be asserted till then.

Self-Refresh

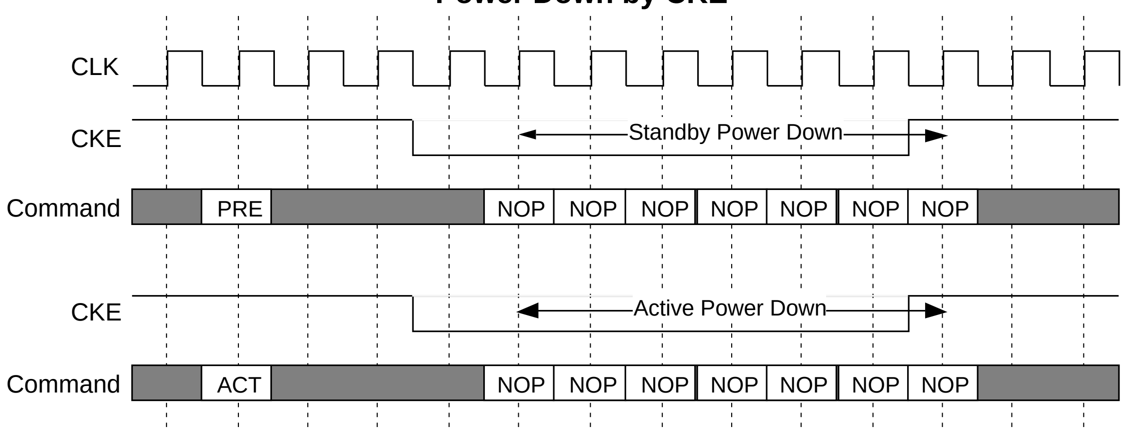


CLK SUSPEND

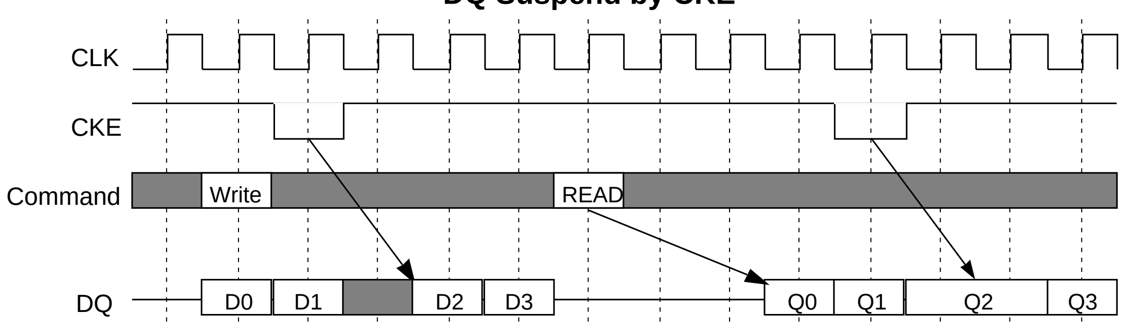
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle. A command at the suspended cycle is ignored.



Power Down by CKE



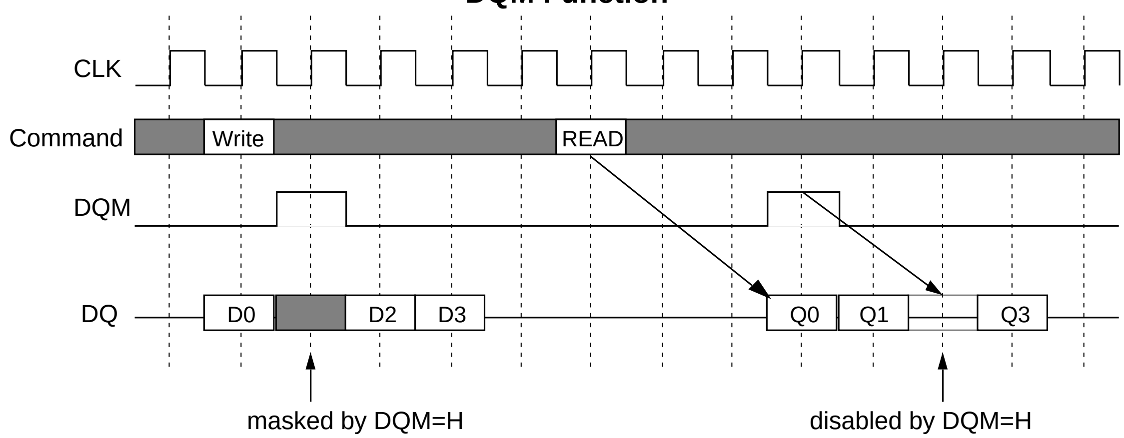
DQ Suspend by CKE



DQM CONTROL

DQM is a dual function signal defined as the data mask for writes and the output disable for reads.
During writes, DQM masks input data word by word. DQM to write mask latency is 0.
During reads, DQM forces output to Hi-Z word by word. DQM to output Hi-Z latency is 2.

DQM Function



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-0.5 ~ 4.6	V
VddQ	Supply Voltage for Output	with respect to VssQ	-0.5 ~ 4.6	V
VI	Input Voltage	with respect to Vss	-0.5 ~ Vdd+0.5	V
VO	Output Voltage	with respect to VssQ	-0.5 ~ VddQ+0.5	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta = 25 °C	1000	mW
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vdd	Supply Voltage	3.0	3.3	3.6	V
Vss	Supply Voltage	0	0	0	V
VddQ	Supply Voltage for Output	3.0	3.3	3.6	V
VssQ	Supply Voltage for Output	0	0	0	V
VIH	High-Level Input Voltage all inputs	2.0		Vdd+0.3	V
VIL	Low-Level Input Voltage all inputs	-0.3		0.8	V

CAPACITANCE

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits (max.)	Unit
CI(A)	Input Capacitance, address pin	VI=Vss	5	pF
CI(C)	Input Capacitance, control pin	f=1MHz	5	pF
CI(K)	Input Capacitance, CLK pin	Vi=25mVrms	5	pF
CI/O	Input Capacitance, I/O pin		7	pF

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, Output Open, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits (max)			Unit
			125 MHz	100 MHz	83 MHz	
Icc1s	operating current, single bank	tRC=min, tCLK=min, BL=1, CL=3	95	85	75	mA
Icc1d	operating current, dual bank	tRC=min, tCLK=min, BL=1, CL=3	130	115	105	mA
Icc2h	standby current, CKE=H	all banks idle, tCLK=min	25	22	20	mA
Icc2l	standby current, CKE=L	all banks idle, tCLK=min	2	2	2	mA
Icc3h	active standby current, CKE=H	all banks active, tCLK=min	50	45	40	mA
Icc3l	active standby current, CKE=L	all banks active, tCLK=min	2	2	2	mA
Icc4	burst current	all banks active, tCLK=min, BL=4, CL=3	130	115	105	mA
Icc5	auto-refresh current	tRC=min, tCLK=min	130	115	105	mA
Icc6	self-refresh current	CKE <0.2v	1	1	1	mA

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits		Unit
			Min.	Max.	
VOH (DC)	High-Level Output Voltage (DC)	IOH=-2mA	2.4		V
VOL (DC)	Low-Level Output Voltage (DC)	IOL= 2mA		0.4	V
IOZ	Off-state Output Current	Q floating VO=0 ~ VddQ	-10	10	µA
I_I	Input Current	VIH = 0 ~ VddQ+0.3V	-10	10	µA

AC TIMING REQUIREMENTS

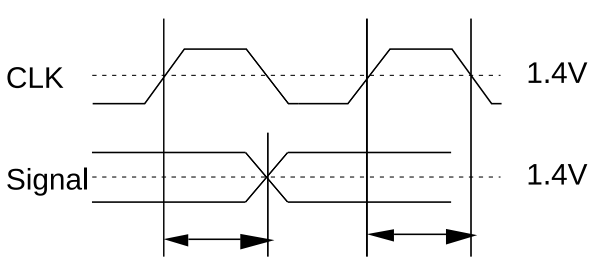
(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Input Pulse Levels: 0.8V to 2.0V

Input Timing Measurement Level: 1.4V

Symbol	Parameter		Limits						Unit	note
			-8		-10		-12			
			Min.	Max.	Min.	Max.	Min.	Max.		
tCLK	CLK cycle time	CL=2	12		15		15		ns	
		CL=3	8		10		12		ns	
tCH	CLK High pulse width		3		4		4		ns	
tCL	CLK Low pulse width		3		4		4		ns	
tT	Transition time of CLK		1	10	1	10	1	10	ns	
tIS	Input Setup time (all inputs)		2		3		3		ns	
tIH	Input Hold time (all inputs)		1		1		1		ns	
tRC	Row Cycle time		80		90		100		ns	
tRCD	Row to Column Delay		24		30		30		ns	
tRAS	Row Active time		56	10000	60	10000	70	10000	ns	
tRP	Row Precharge time		24		30		30		ns	
tWR	Write Recovery time		10		10		12		ns	
tRRD	Act to Act Delay time		16		20		24		ns	1
tCCD	Col to Col Delay time		8		10		12		ns	
tRSC	Mode Register Set Cycle time		16		20		24		ns	
tSRX	Self Refresh Exit time		8		10		12		ns	
tREF	Refresh Interval time			64		64		64	ms	

Note:1 2 ACT commands are allowed within tRC.



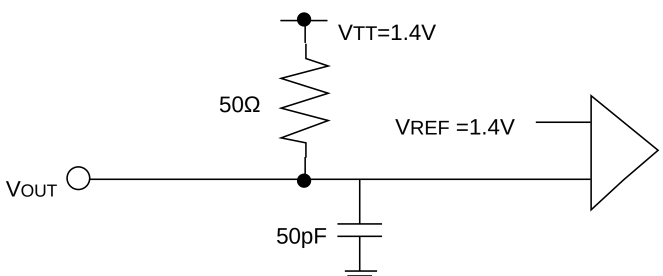
Any AC timing is referenced to the input signal crossing through 1.4V.

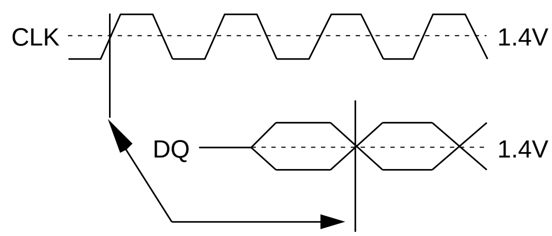
SWITCHING CHARACTERISTICS

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

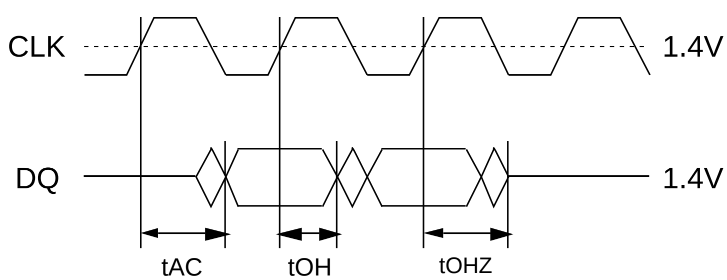
Symbol	Parameter		Limits -8 Min.	-8 Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
tAC	Access time from CLK	CL=2		8		9		9.5	ns
		CL=3		6		8		8	ns
tOH	Output Hold time from CLK	CL=2	2.5		3		3		ns
		CL=3	2.5		3		3		
tOLZ	Delay time, output low impedance from CLK		0		0		0		ns
tOHZ	Delay time, output high impedance from CLK		2.5	7	3	8	3	8	ns

Output Load Condition

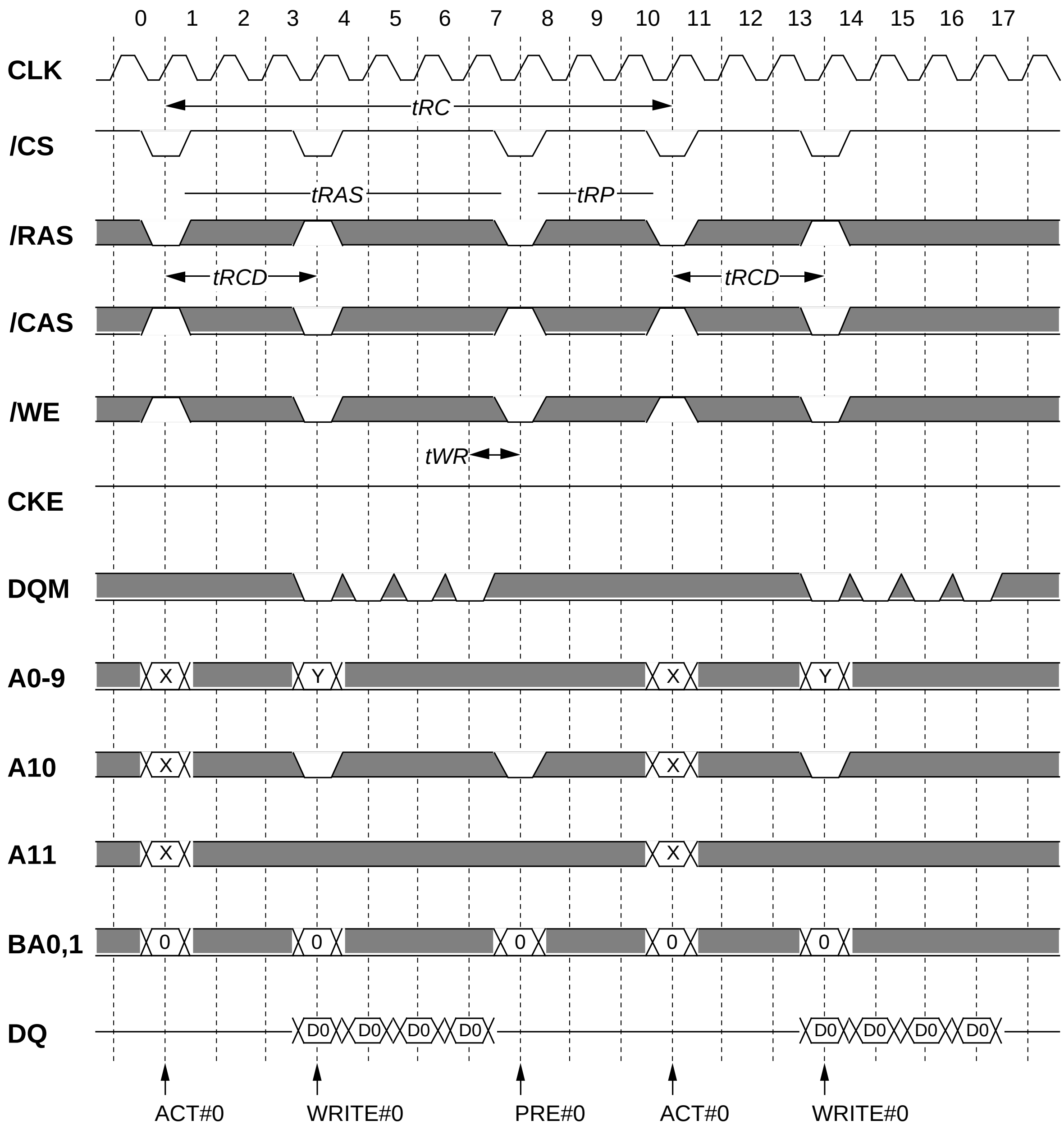




Output Timing Measurement Reference Point

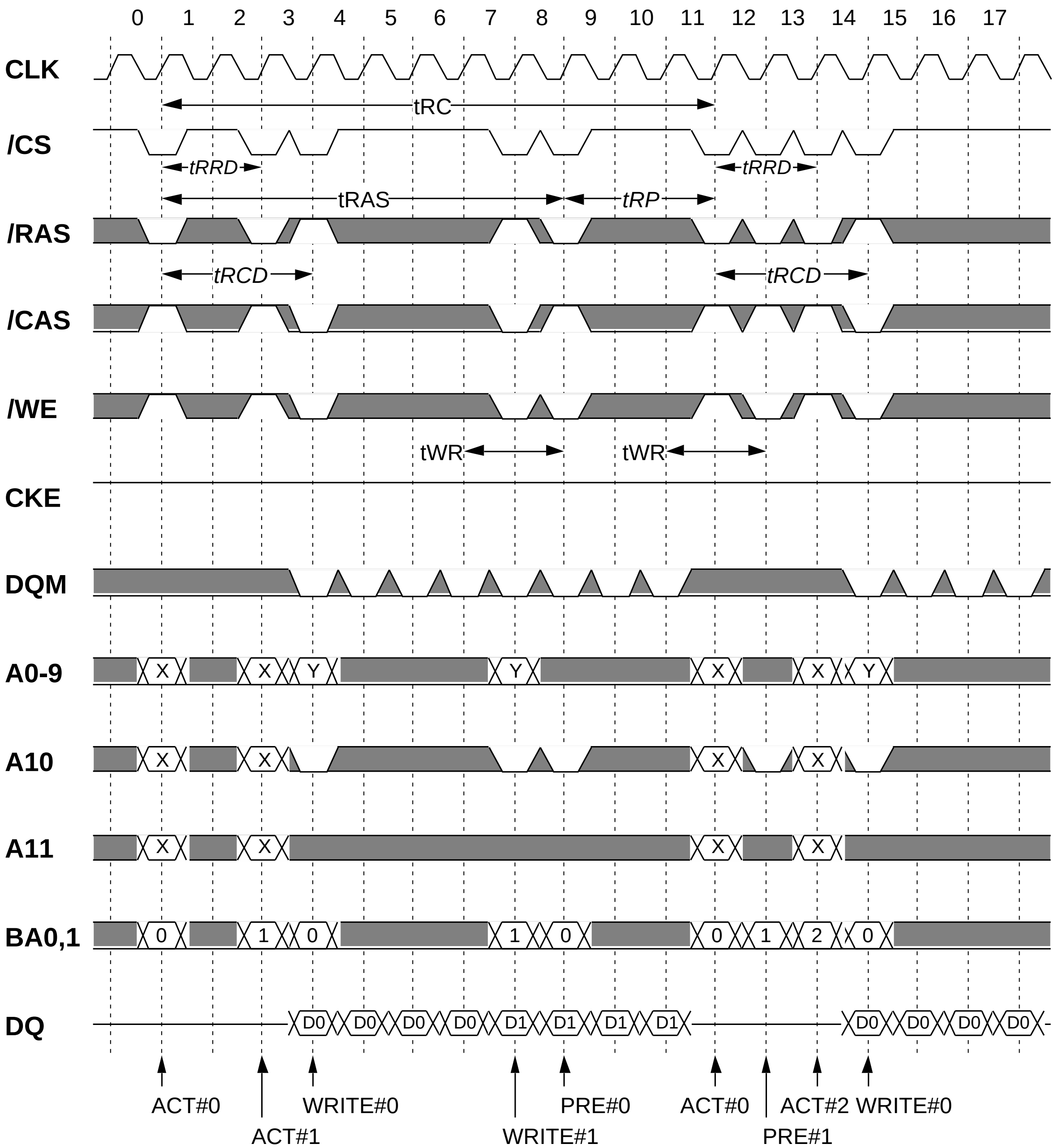


Burst Write (single bank) @BL=4



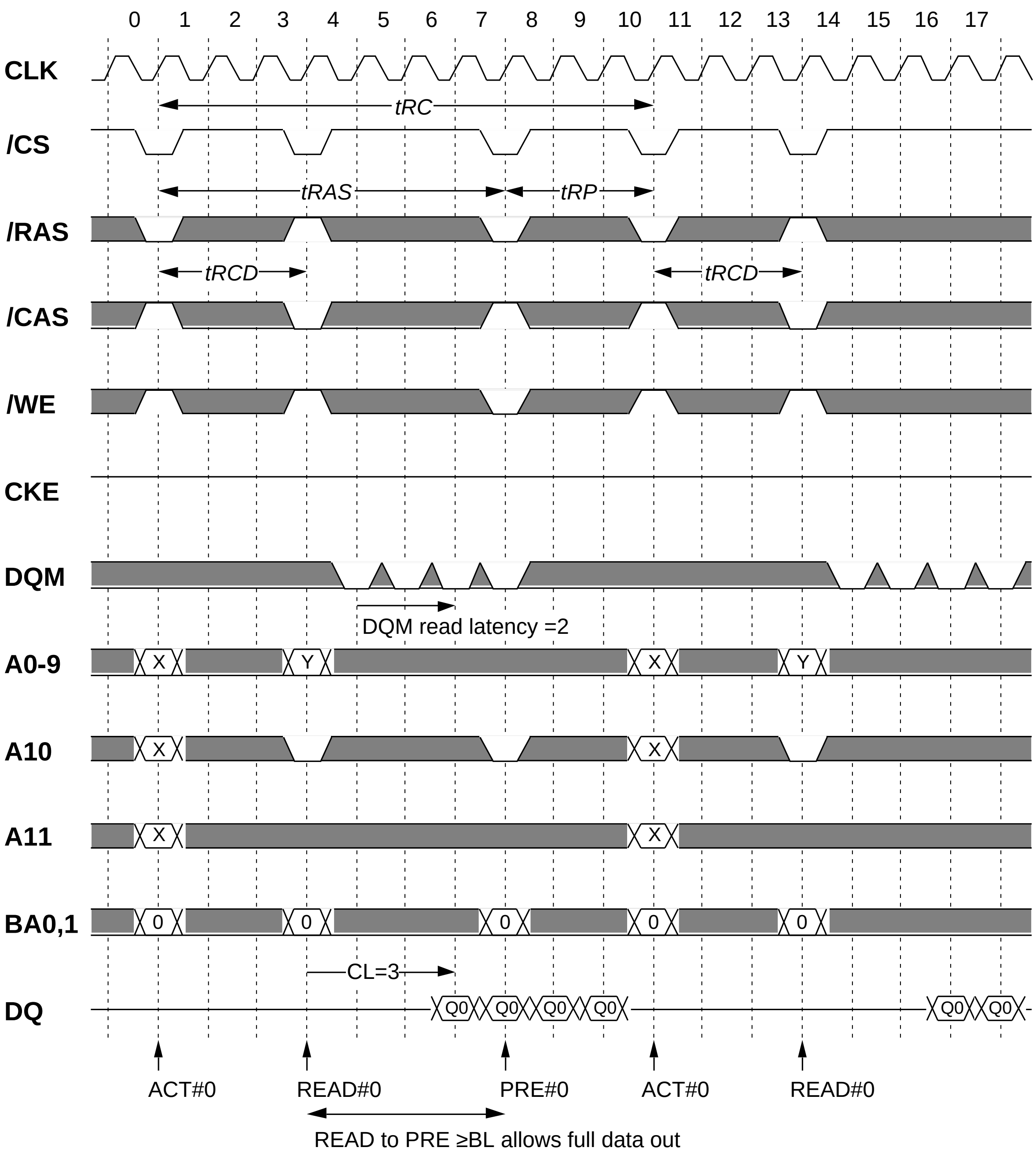
Italic parameter indicates minimum case

Burst Write (multi bank) @BL=4



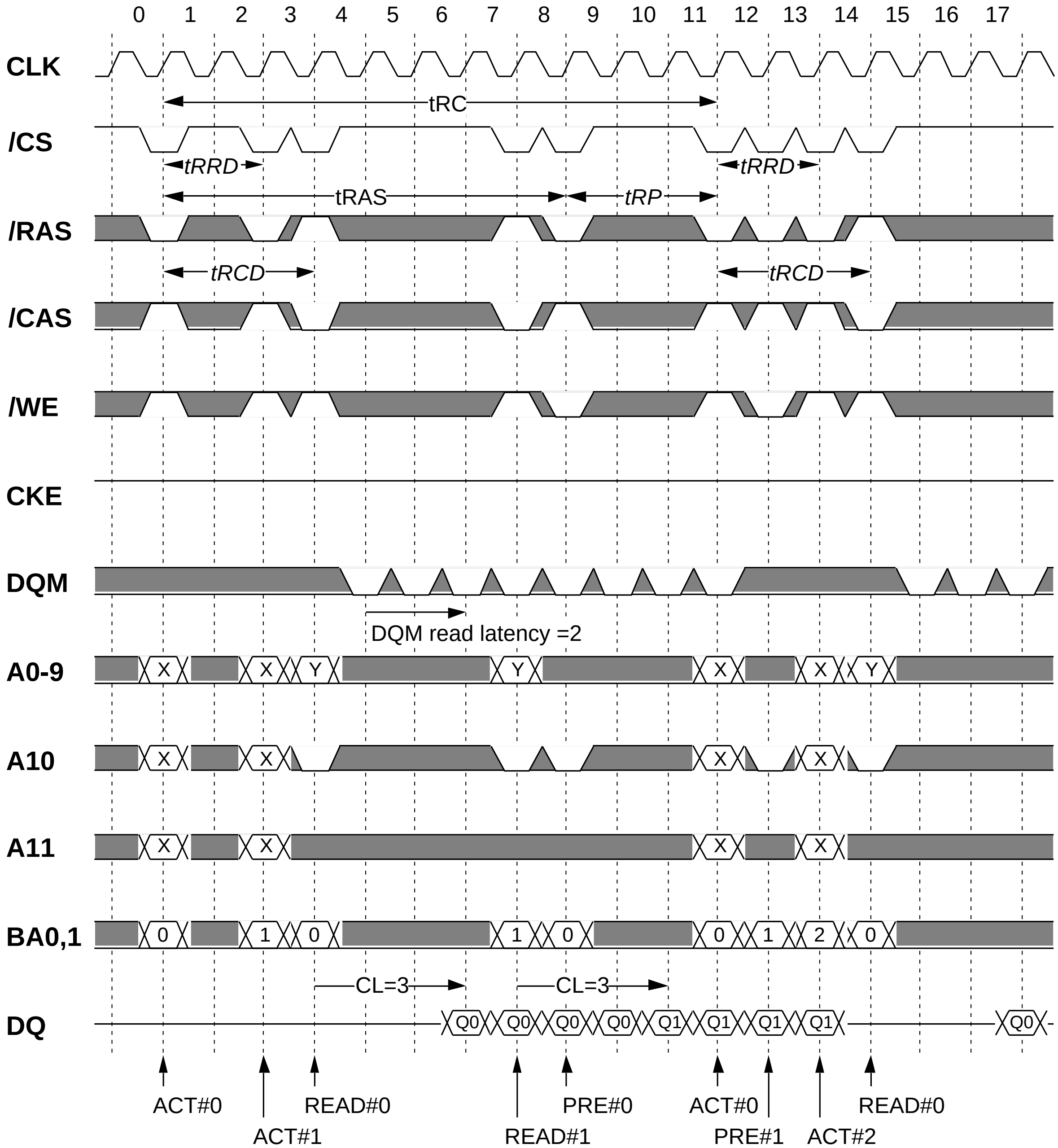
Italic parameter indicates minimum case

Burst Read (single bank) @BL=4 CL=3



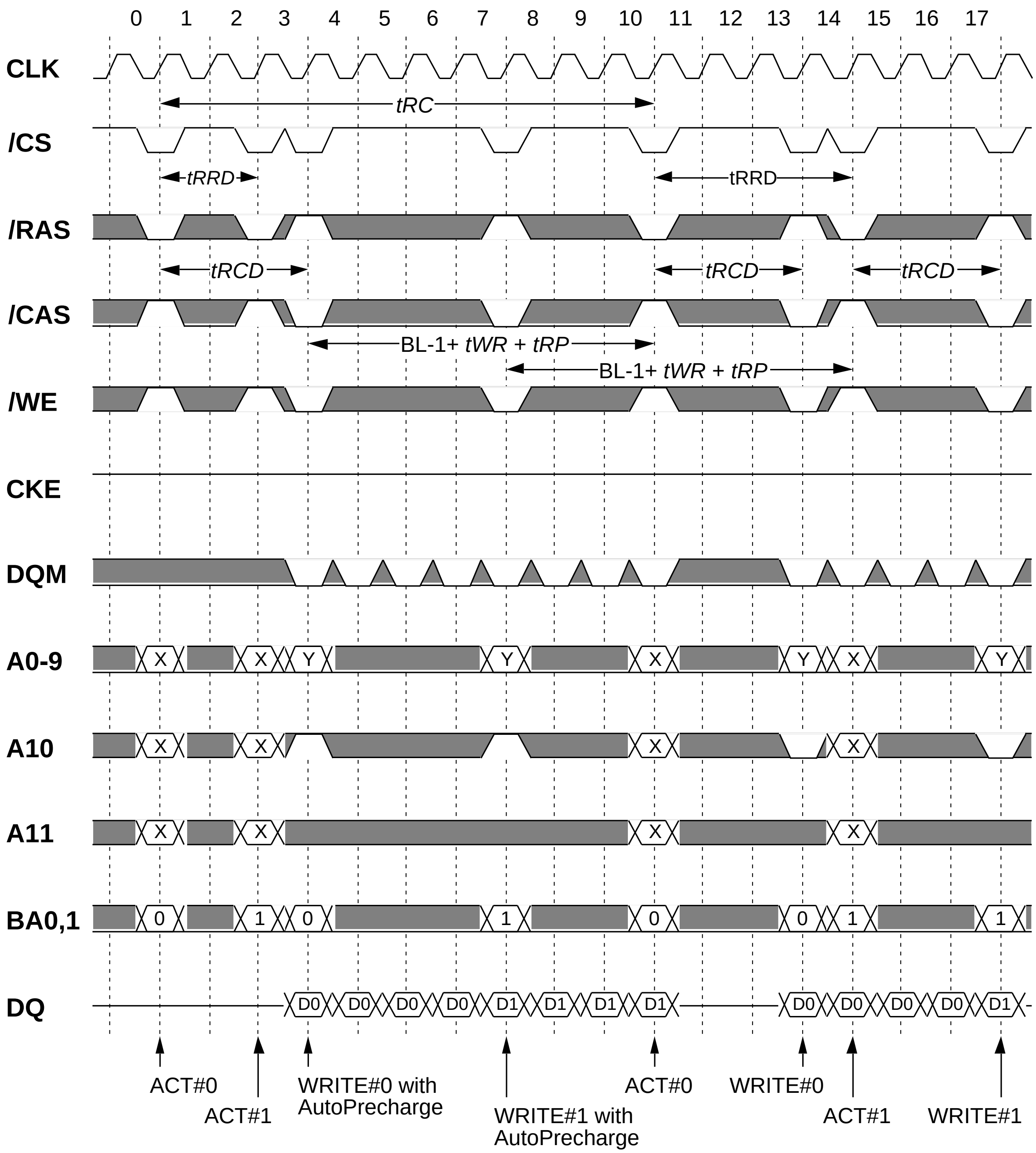
Italic parameter indicates minimum case

Burst Read (multiple bank) @BL=4 CL=3



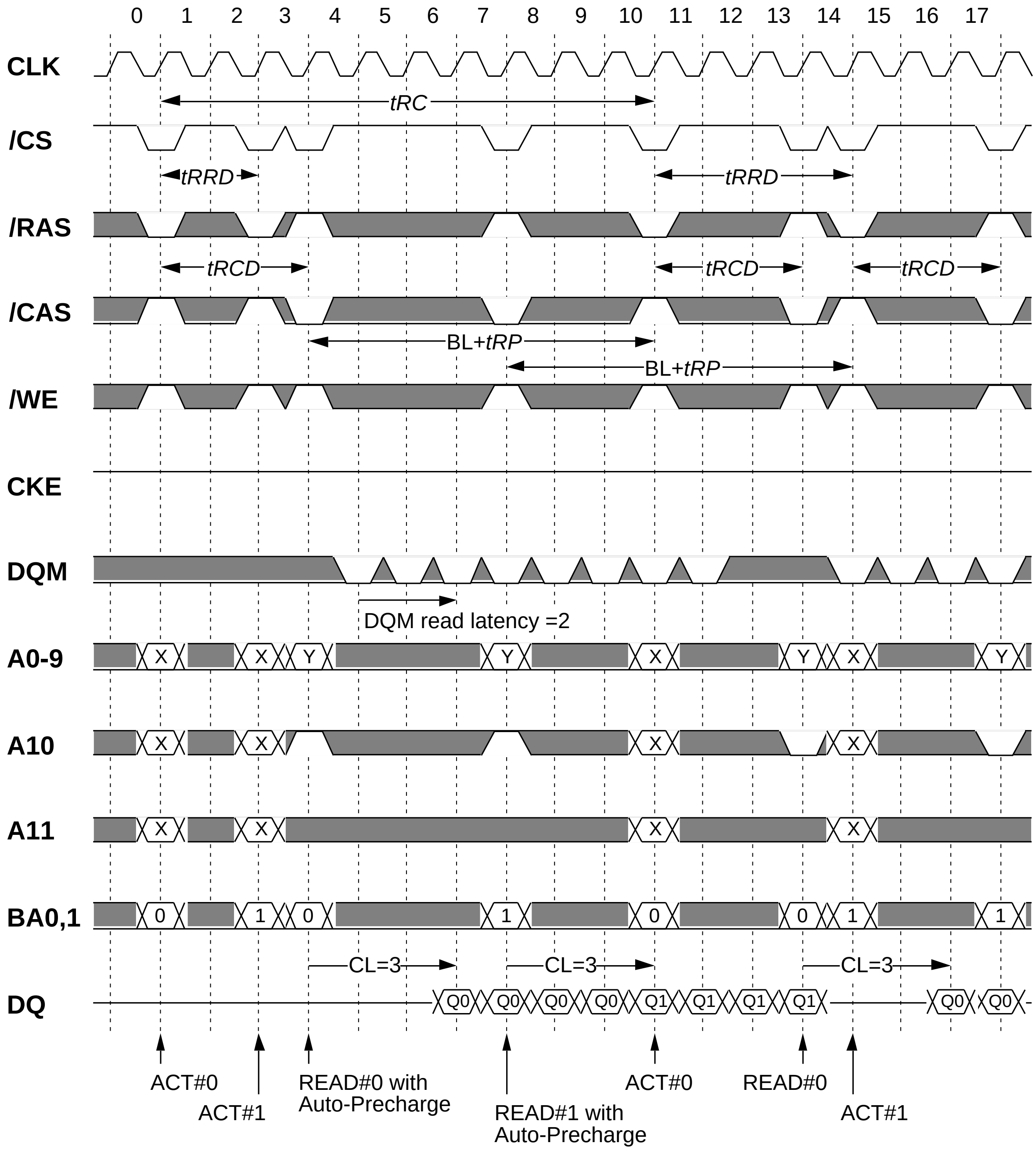
Italic parameter indicates minimum case

Burst Write (multi bank) with Auto-Precharge @BL=4



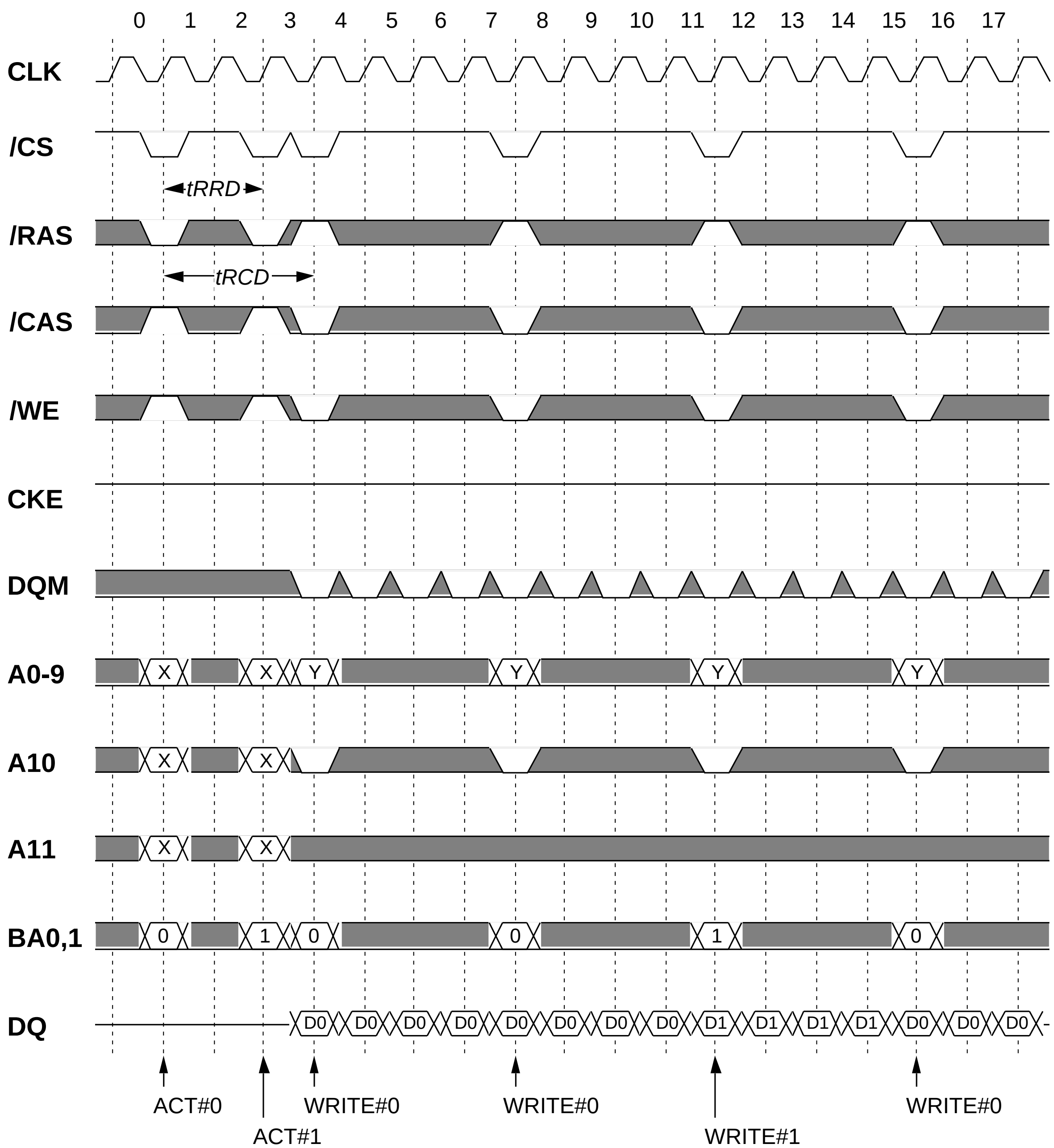
Italic parameter indicates minimum case

Burst Read (multiple bank) with Auto-Precharge @BL=4 CL=3



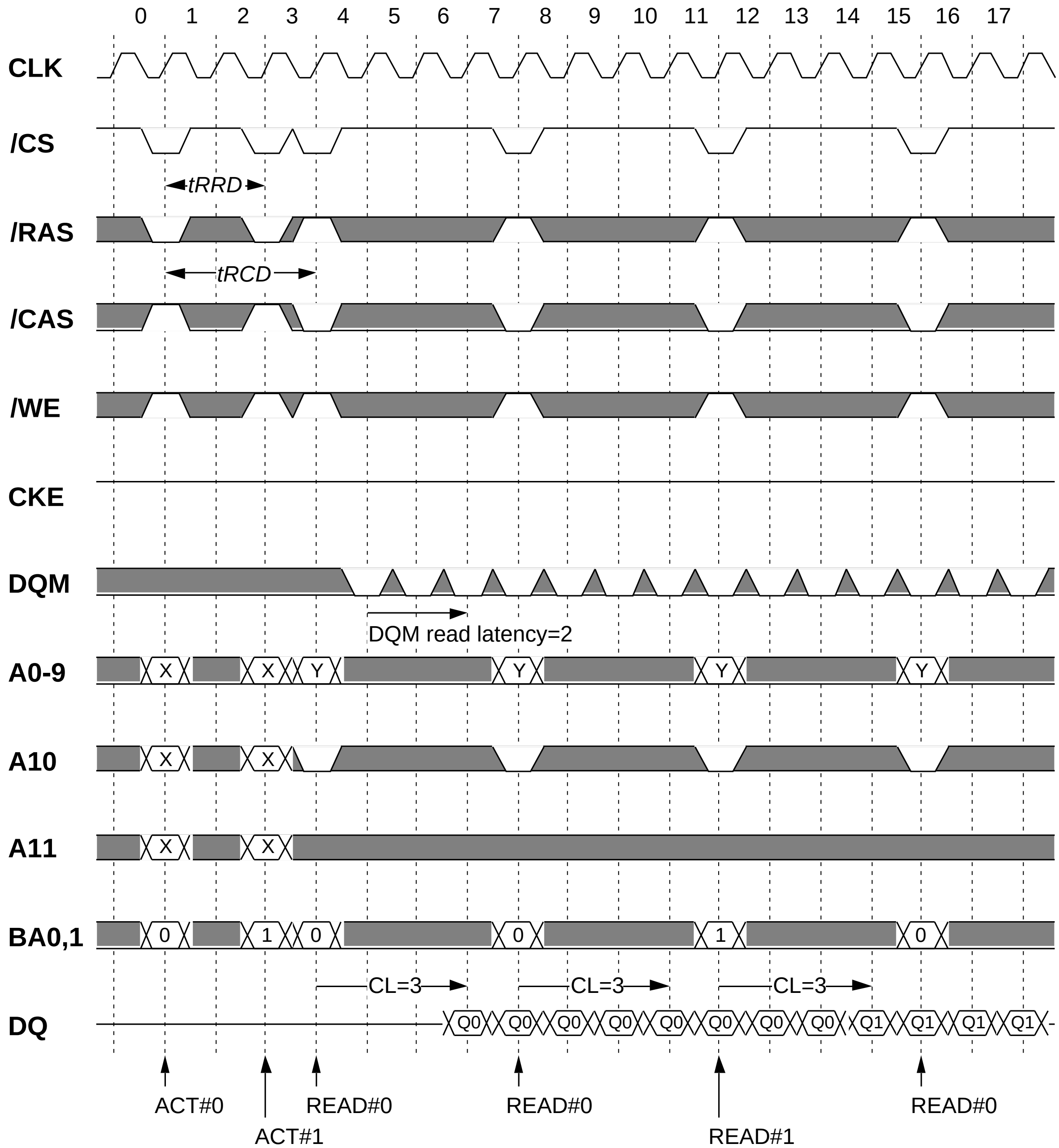
Italic parameter indicates minimum case

Page Mode Burst Write (multi bank) @BL=4



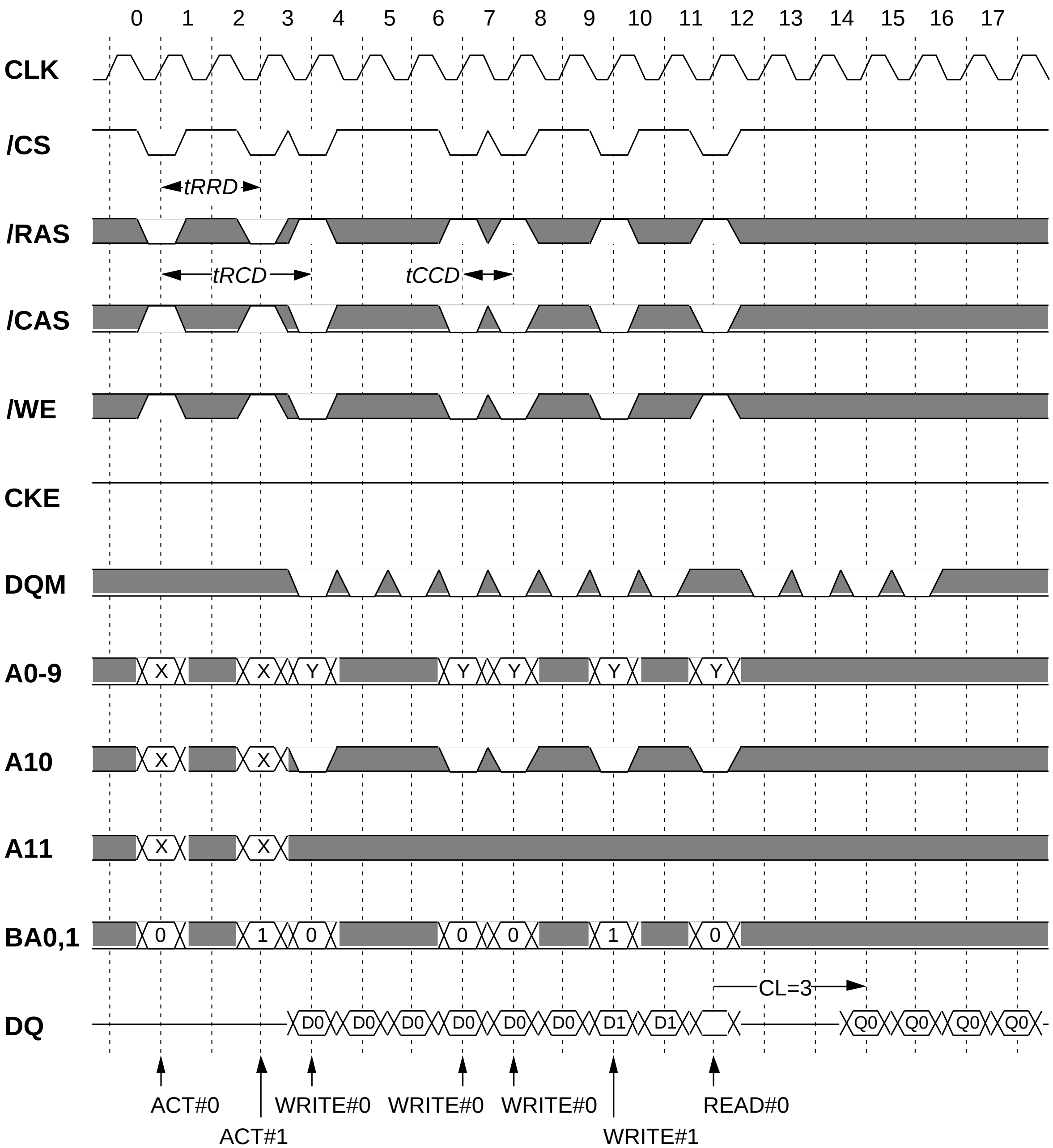
Italic parameter indicates minimum case

Page Mode Burst Read (multi bank) @BL=4 CL=3



Italic parameter indicates minimum case

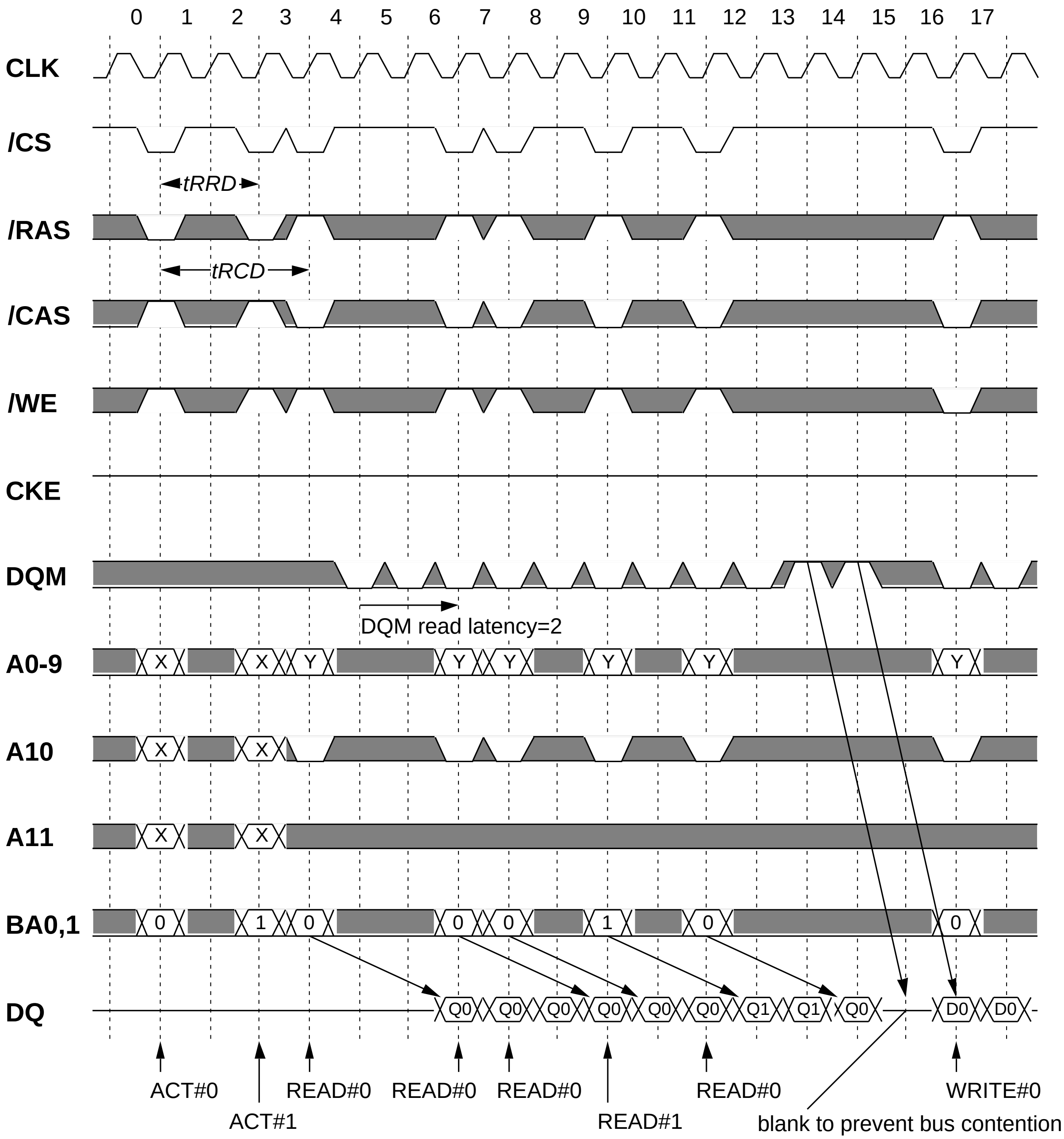
Write Interrupted by Write / Read @BL=4



Burst Write can be interrupted by Write or Read of any active bank.

Italic parameter indicates minimum case

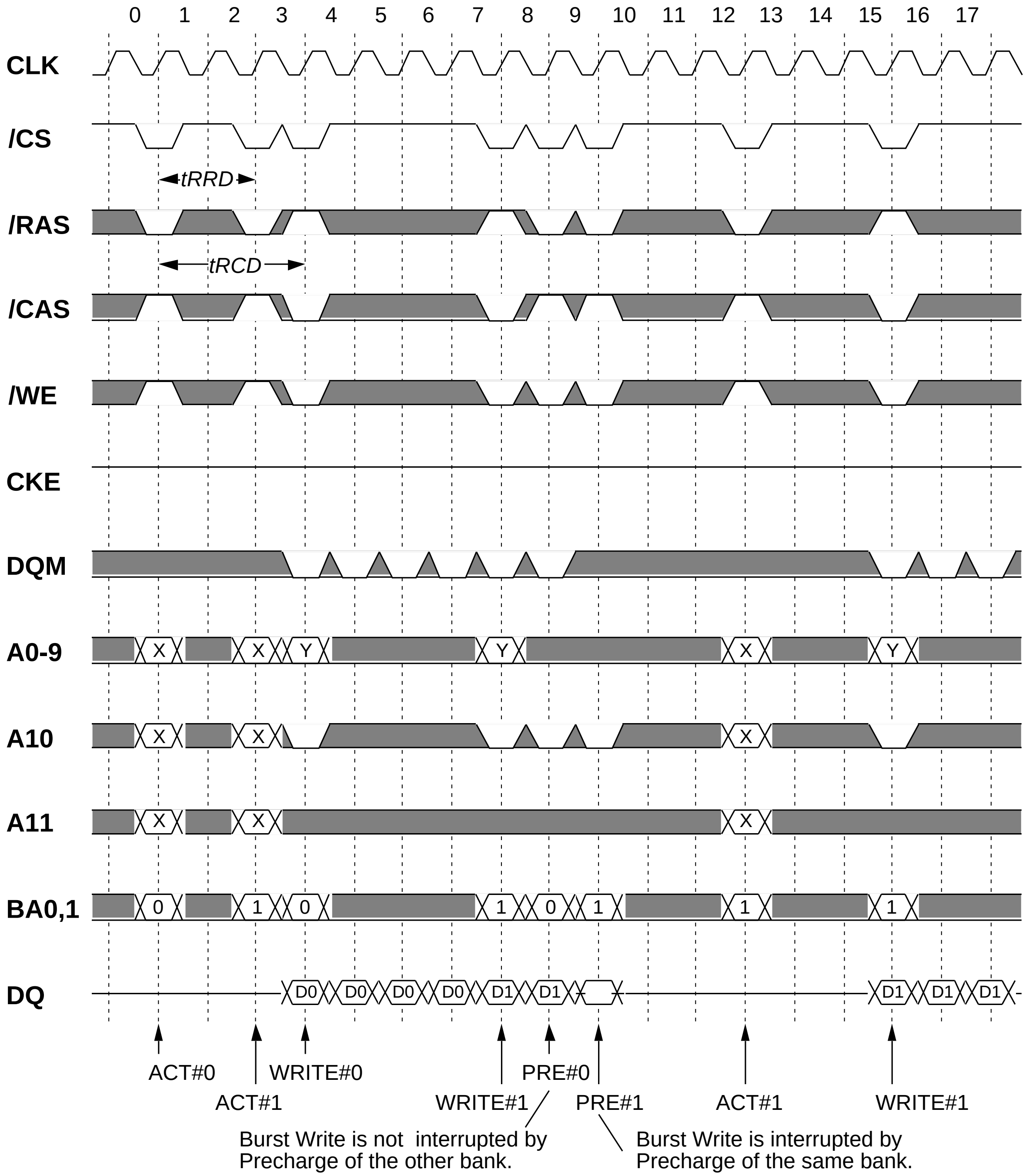
Read Interrupted by Read / Write @BL=4 CL=3



Burst Read can be interrupted by Read or Write of any active bank.

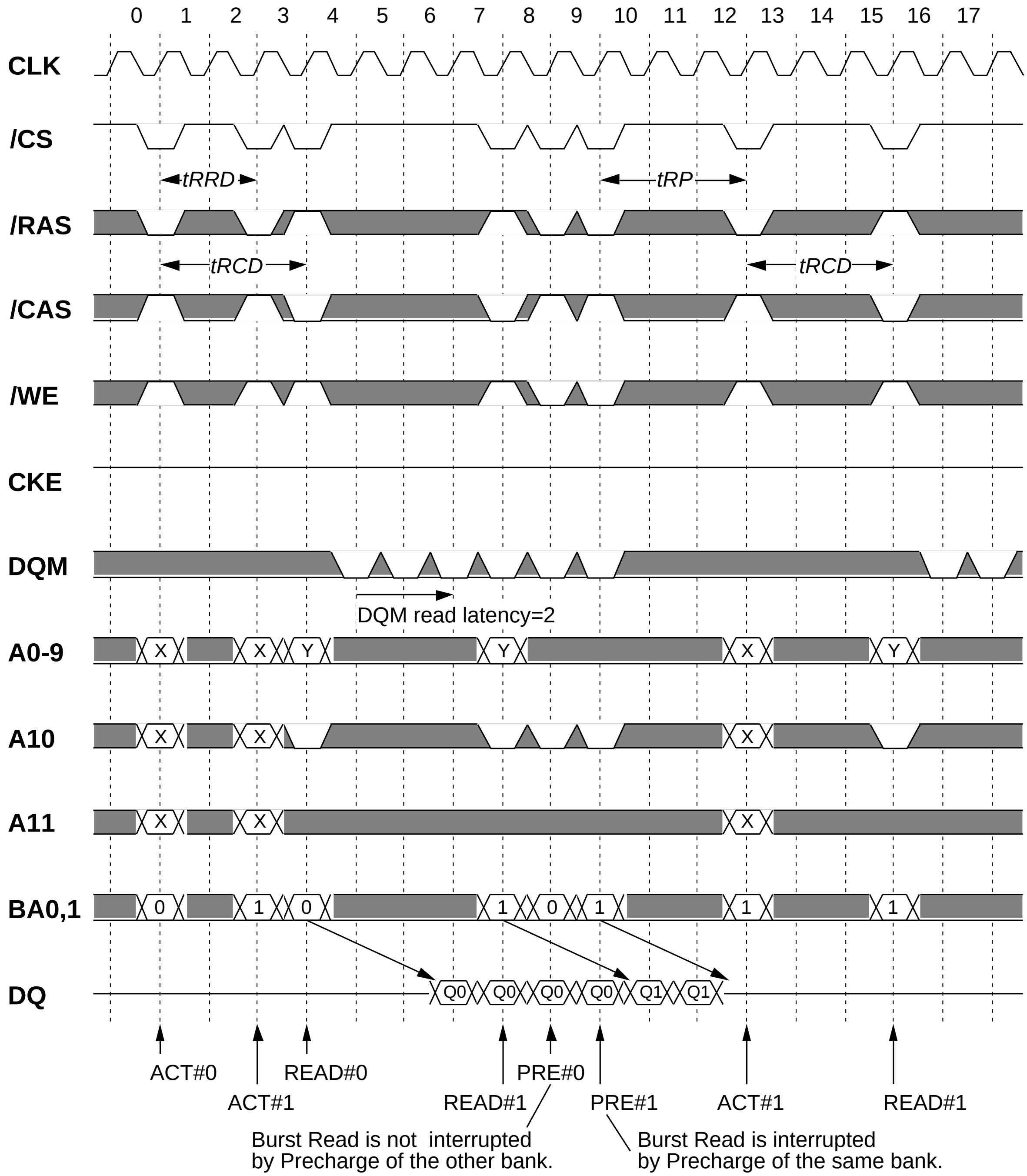
Italic parameter indicates minimum case

Write Interrupted by Precharge @BL=4



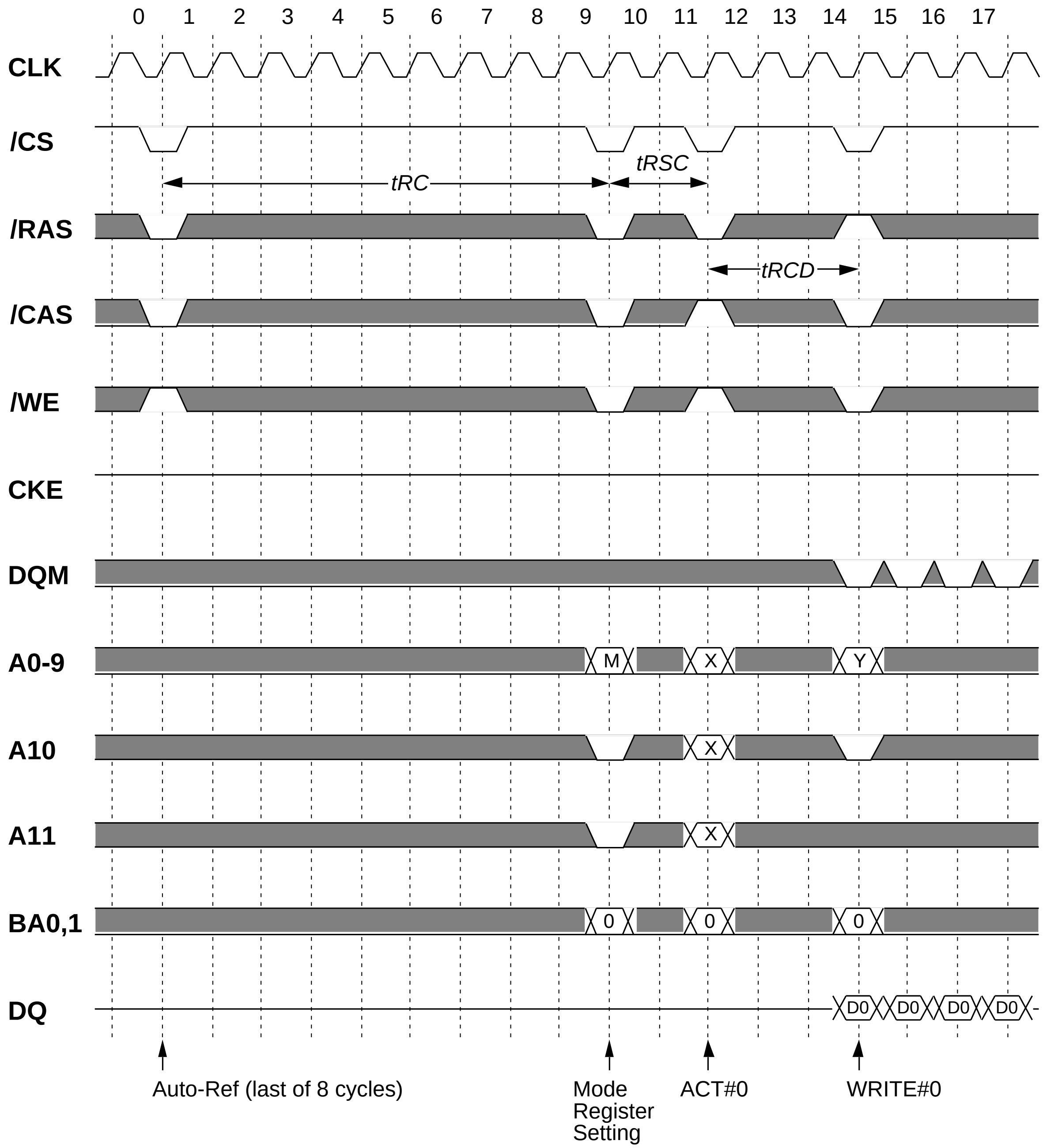
Italic parameter indicates minimum case

Read Interrupted by Precharge @BL=4 CL=3



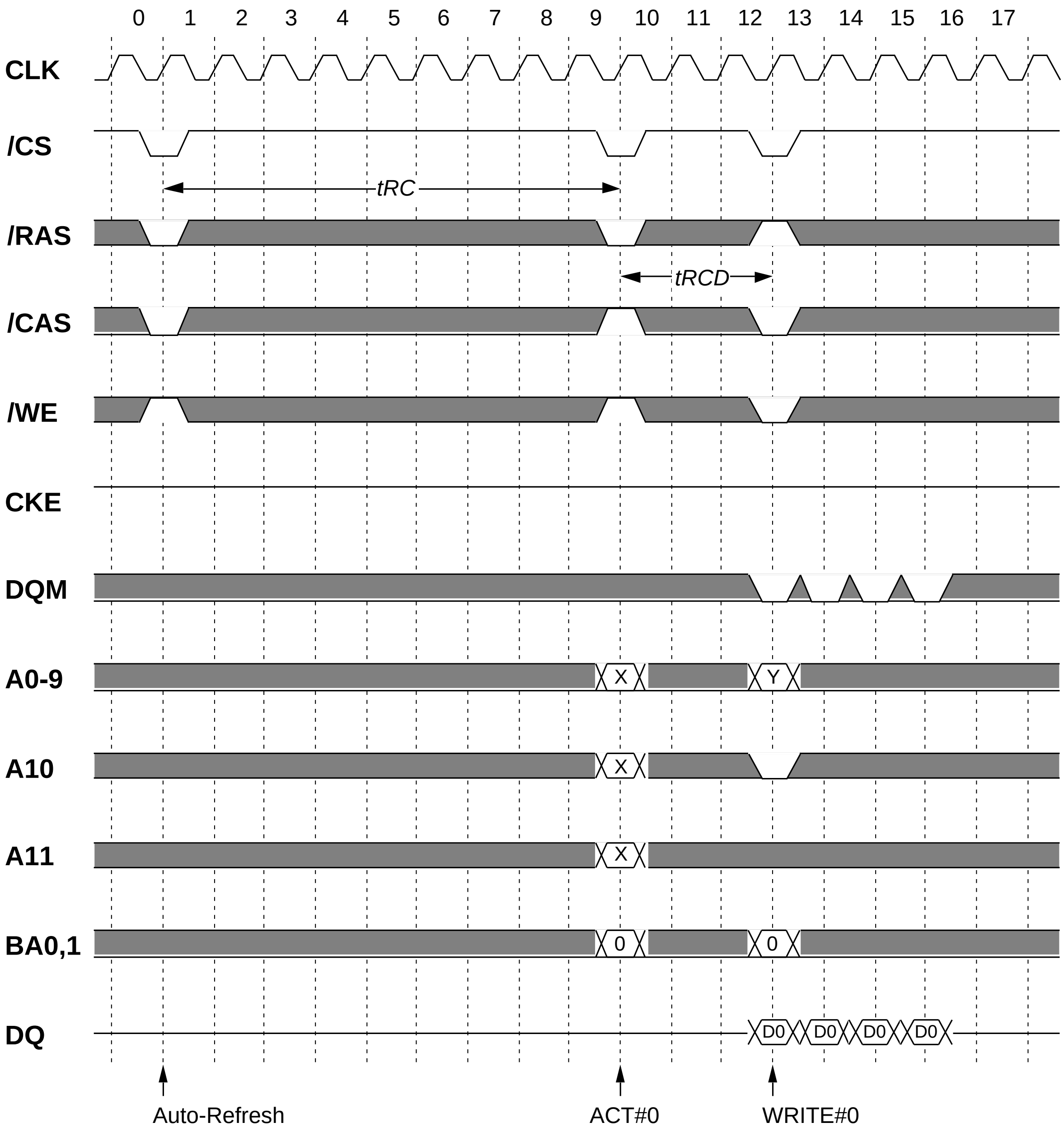
Italic parameter indicates minimum case

Mode Register Setting



Italic parameter indicates minimum case

Auto-Refresh @BL=4

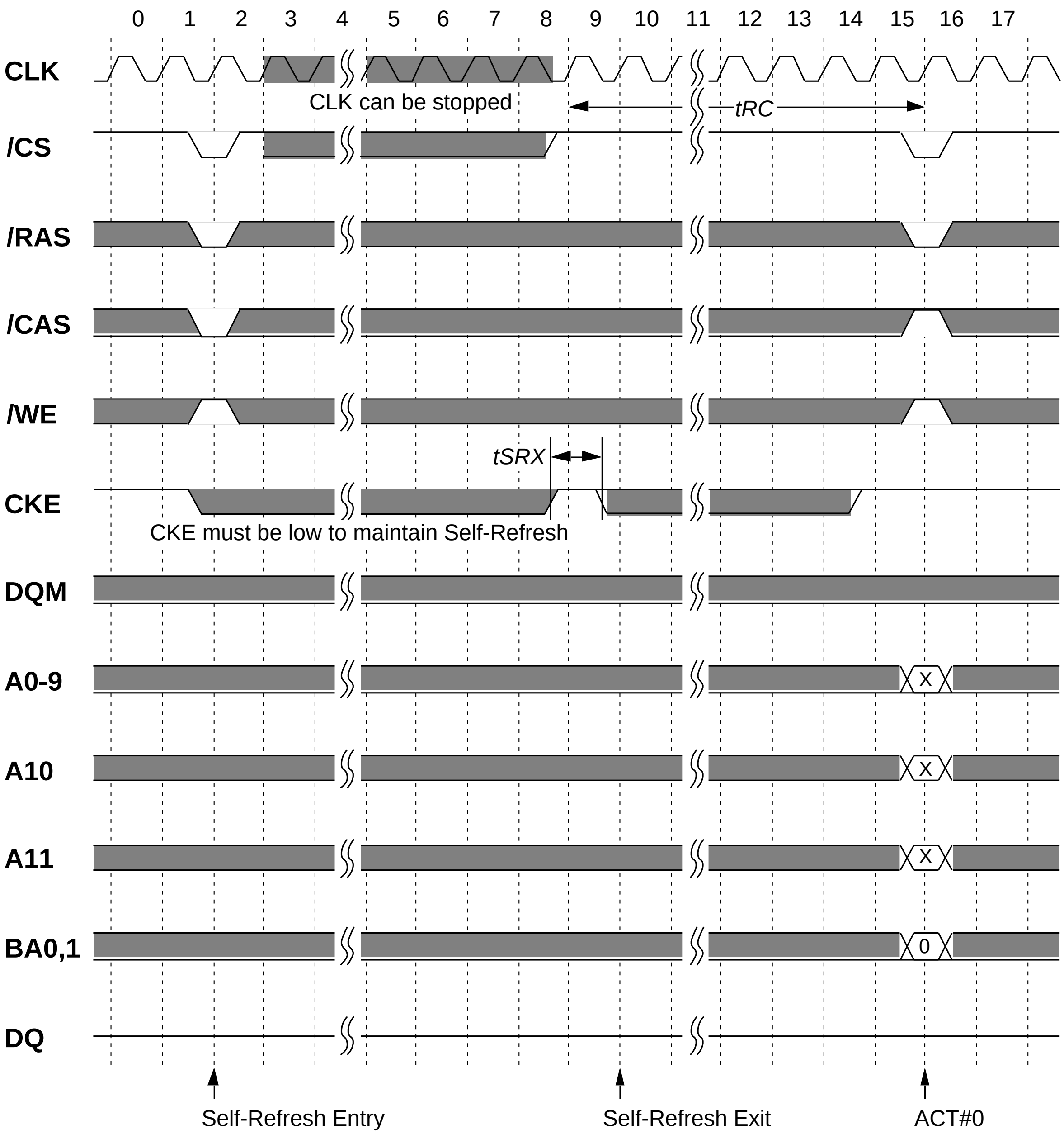


Before Auto-Refresh,
all banks must be idle state.

After tRC from Auto-Refresh,
all banks are idle state.

Italic parameter indicates minimum case

Self-Refresh

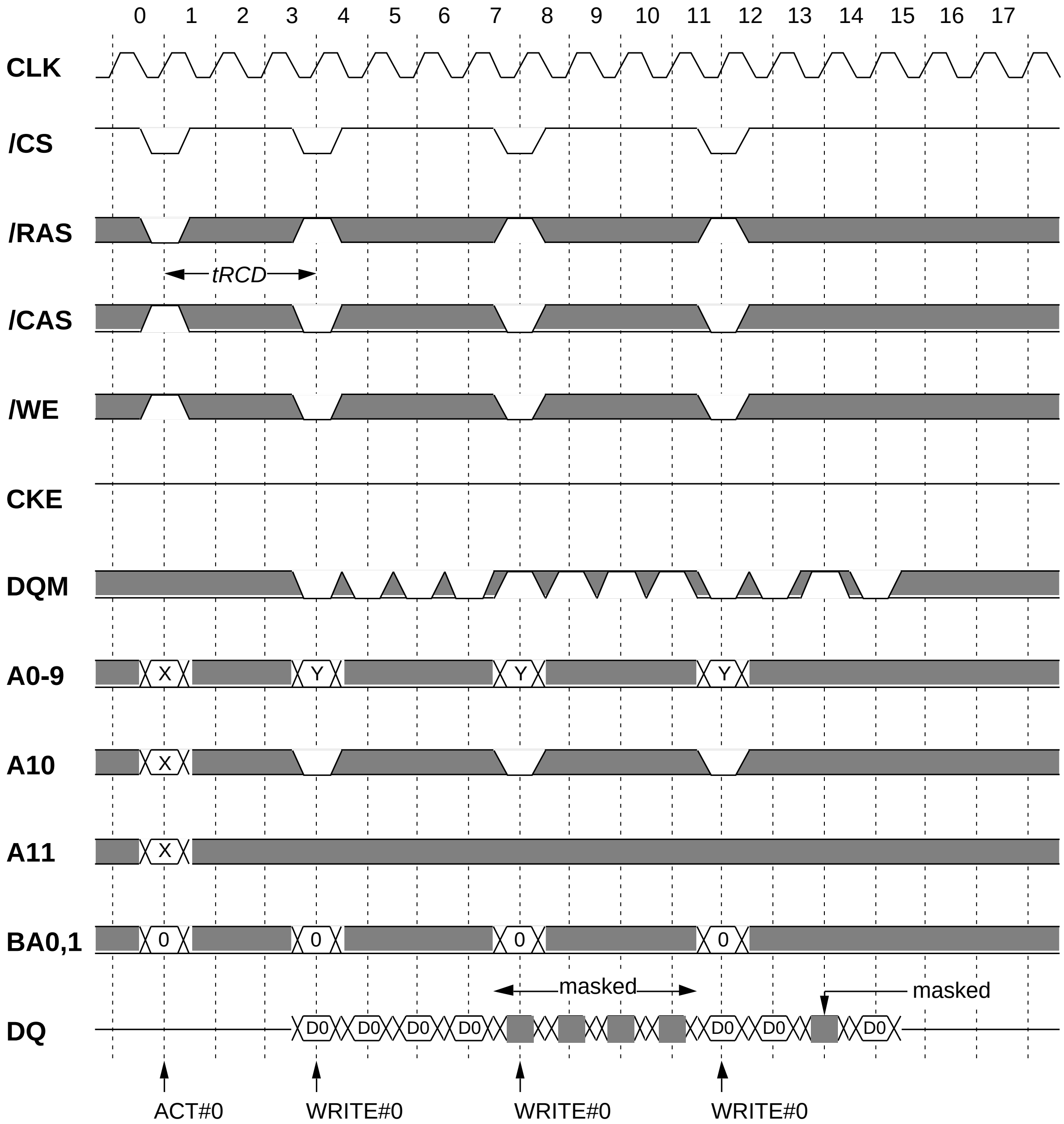


Before Self-Refresh Entry,
all banks must be idle state.

After tRC from Self-Refresh Exit,
all banks are idle state.

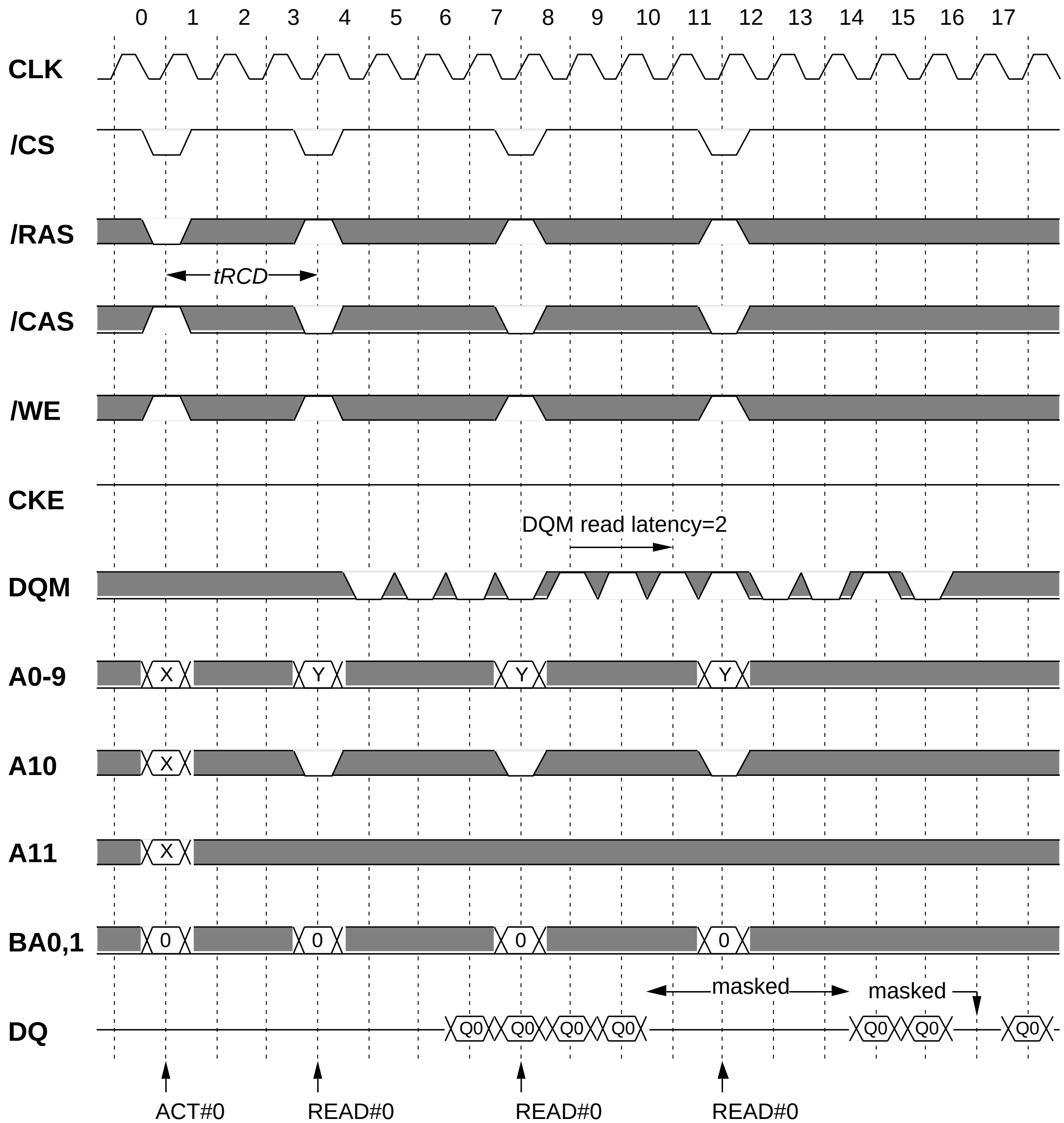
Italic parameter indicates minimum case

DQM Write Mask @BL=4



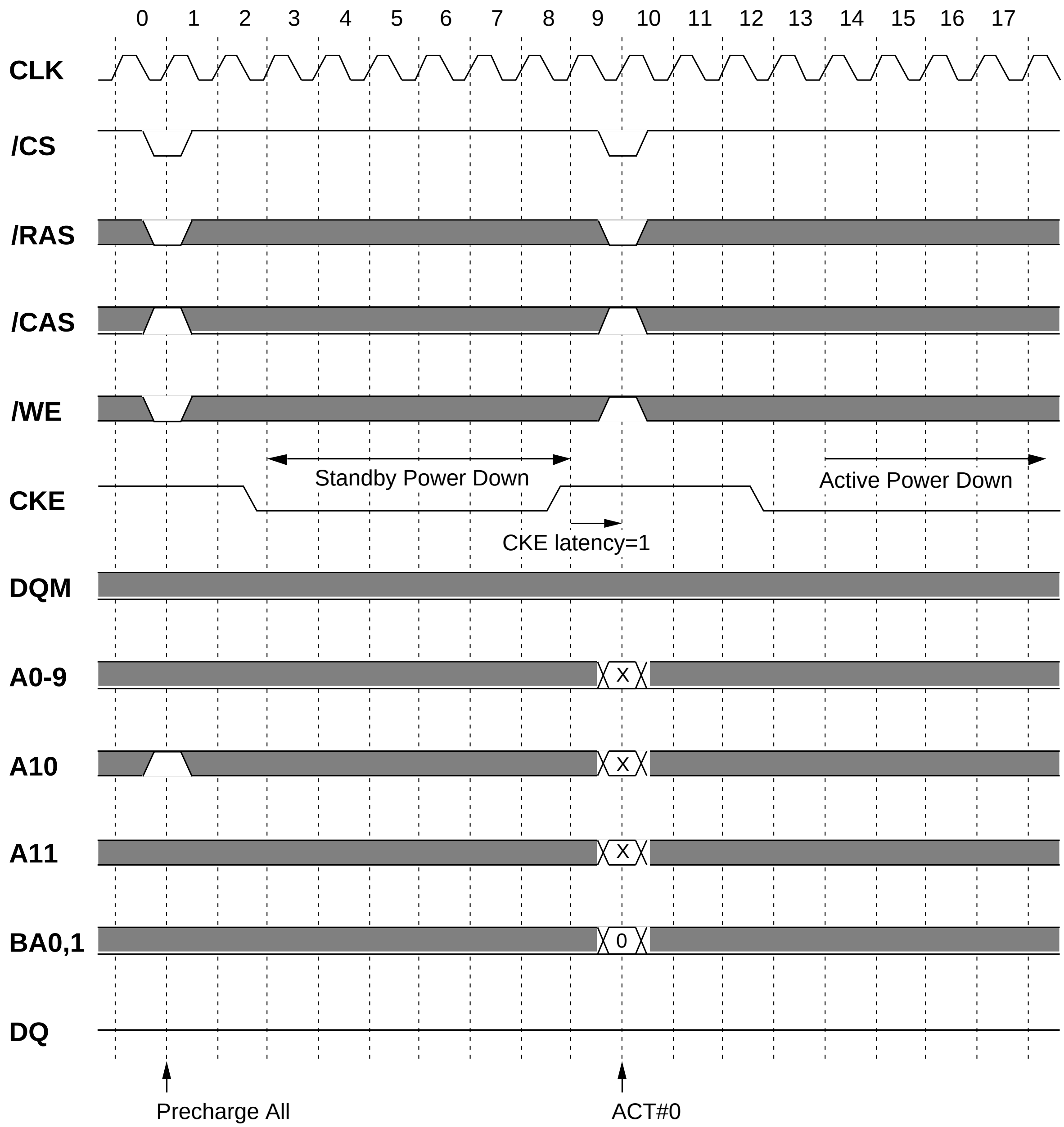
Italic parameter indicates minimum case

DQM Read Mask @BL=4 CL=3



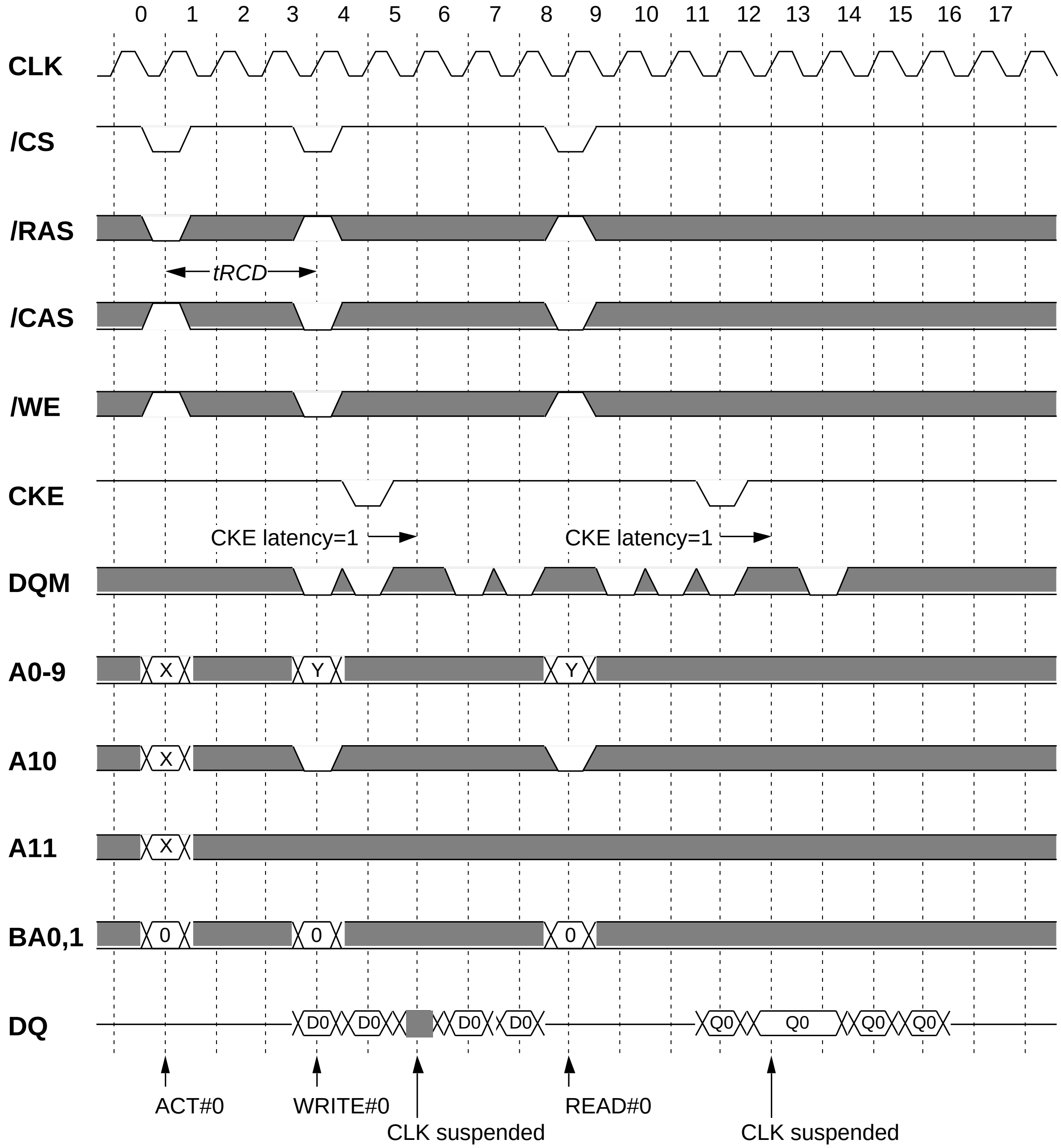
Italic parameter indicates minimum case

Power Down



Italic parameter indicates minimum case

CLK Suspend @BL=4 CL=3



Italic parameter indicates minimum case